

# THE ENERGY BALANCE ERROR FOR CIRCUIT TRANSIENT ANALYSIS

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Two algorithms for the time step choice implemented in circuit simulators are analyzed. A new error and a new time step choice algorithm are proposed. An example is given for illustration.

## 1. INTRODUCTION

The time step magnitude in transient analysis of electrical circuits is chosen depending on certain errors. In SPICE-like circuit simulators (SPICE, PSPICE, HSPICE, SPECTRE, SPECTRE RF) the local truncation error (LTE) is used for each state variable and its time derivative. The LTE is estimated in the worst case corresponding to a relative error and to an absolute error. For example, the error of the time derivative of a state variable is:

$$\varepsilon_x = \varepsilon_r \cdot \max\left(\left|\frac{\dot{x}_{n+1}}{x_{n+1}}\right|, \left|\frac{\dot{x}_n}{x_n}\right|\right) + \varepsilon_a \quad (1)$$

where  $\dot{x}_{n+1}$  is the current through a capacitor or the voltage of an inductor. A similar error is defined for  $x_{n+1}$ .

For each time step, the maximum allowed LTE is given by:

$$E = \max(\varepsilon_x, \varepsilon_{\dot{x}}) \quad (2)$$

Starting from this value, a maximum time step is computed as:

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$$h_{n+1} \leq \sqrt{6E / \left| \frac{d^3 x_n}{dt^3} \right|} \quad (3)$$

This algorithm for time step computation can be outlined as follows [1]:

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 $t_{n+1} = t_n + h_n$ 
solve for  $t_{n+1}$ 
if  $iter\_num < ITL4$ 
compute  $h_{n+1} = f(LTE)$ 
  if  $h_{n+1} < 0.9 \cdot h_n$  then
    reject  $t_{n+1}$ 
     $h_n = h_{n+1}$ 
    compute for the new  $t_{n+1}$ 
  else
    accept  $t_{n+1}$ 
     $h_{n+1} = \min(h_{n+1}, 2 \cdot h_n, TMAX)$ 
    continue with  $t_{n+2}$ 
else
  reject  $t_{n+1}$ 
   $h_n = h_n / 8$ 
  reduce integration order to 1 (BE)
  if ( $h_n > h_{min}$ ) then
    compute for the new  $t_{n+1}$ 
  else print TIME STEP TOO SMALL; analysis is aborted

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where the integration method is trapezoidal and can be changed to backward Euler (BE), TMAX is the final time,  $iter\_num$  is the current iteration number and  $ITL4$  is the maximum iteration number.

The main drawback of this algorithm is the relation (3) which is based on the remainder estimation in Taylor formula [2]. The LTE of the trapezoidal algorithm

is estimated as  $-\frac{h^3}{12} x'''(\tau)$  where  $\tau$  is an unknown value in the vicinity of  $t_{n+1}$ .

Moreover, the third derivative must be approximated knowing only the sample values given by a numerical method (the form of the solution between samples is not known).

Another algorithm for time step choice, based on an energy error, is proposed in [3]. The energy accumulated by a nonlinear capacitor in the time step  $[t_j, t_{j+1}]$  can be computed exactly as:

$$E_{j+1} - E_j = \int_{v_j}^{v_{j+1}} \frac{dq}{dv} v dv \quad (4)$$

where  $q$  is the capacitor charge,  $v_j$  is the capacitor voltage at  $t_j$  and  $v_{j+1}$  is the capacitor voltage at  $t_{j+1}$ .

For this capacitor, the energy balance in this time step is the difference between the accumulated energy and the energy fed by circuit into capacitor:

$$\Delta E = E_{j+1} - E_j - \int_{t_j}^{t_{j+1}} i(\tau)v(\tau)d\tau \quad (5)$$

where  $i$  is the capacitor current.

If  $\Delta E \neq 0$ , the integration algorithm gives an erroneous estimate of the solution. Obviously  $\lim_{h_{j+1} \rightarrow 0} \Delta E = 0$ .

While the accumulated energy depends only on  $v_j$  and  $v_{j+1}$ , the energy fed by circuit into capacitor depends on the functions  $i(\tau)$  and  $v(\tau)$  also.

An algorithm for the computation of the time step based on  $\Delta E$  control is developed in [3]. The maximum allowed  $\Delta E_{j+1}$  in the time interval  $[t_j, t_{j+1}]$  is computed in a similar manner to (1):

$$|\Delta E_{j+1}| < \epsilon_r |\Delta E_j| + \epsilon_a \quad (6)$$

The time step  $h_{j+1}$  is computed solving an optimization problem whose constraints are the relations (6) for all dynamic elements and  $h_{j+1} > 0$ . The actual implementation of this algorithm in the circuit simulator PAN [4] uses a ‘‘cut and try’’ mechanism similar to the SPICE one [5].

Some tests on benchmark circuits proved that PAN transient analysis can be up to an order of magnitude faster than that of SPICE or SPECTRE [6]. There are two reasons explaining these results:

1. The LTE approach is aimed to control the error with which the circuit state equations  $\dot{x} = Ax + b(t)$  are verified, but  $A$  and  $b(t)$  are not available in a circuit simulator; that’s why the SPICE approach imposes some errors for the computation of all magnitudes  $x$  and  $\dot{x}$  without any connection to their weightings given by  $A$  and which are related to the circuit structure; the energy balance for each dynamic

circuit element is more efficient because it takes partially into account the circuit structure.

2. The numerical evaluation of third order derivatives can lead to erroneous results, which, in turn, can force the algorithm to choose smaller values of the time step than are really needed to verify circuit equations.

The main idea of this paper is to go further taking totally into account the circuit structure and using the energy balance error for the whole circuit. This approach is discussed in Section 2, together with an algorithm for the time step choice. An example is presented Section 3, while Section 4 contains conclusions and future work.

## 2. ENERGY BALANCE ERROR AND CHOICE OF THE TIME STEP

For each dynamic element the energy fed into it is defined so that for a linear capacitor we have:

$$E_C = \int_{t_n}^{t_{n+1}} u(\tau) \cdot i(\tau) d\tau = \int_{t_n}^{t_{n+1}} u(\tau) \cdot C \frac{du(\tau)}{d\tau} d\tau = \int_{u(t_n)}^{u(t_{n+1})} C \cdot u du = \frac{C}{2} [u^2(t_{n+1}) - u^2(t_n)] \quad (7)$$

and for a linear inductor we have:

$$E_L = \int_{t_n}^{t_{n+1}} u(\tau) \cdot i(\tau) d\tau = \int_{t_n}^{t_{n+1}} L \frac{di(\tau)}{d\tau} \cdot i(\tau) d\tau = \int_{i(t_n)}^{i(t_{n+1})} L \cdot i di = \frac{L}{2} [i^2(t_{n+1}) - i^2(t_n)] \quad (8)$$

A numerical method gives only the sample values for certain values of time, the form of the function between samples being unknown. To compute the energy fed into resistors and sources, their voltages and currents are considered as linear or quadratic functions of time in the interval  $[t_j, t_{j+1}]$ . This approximation can lead to errors in energy computation.

The absolute energy balance error is defined as:

$$\Delta E_a = \sum_{k=1}^n E_k \quad (9)$$

and the relative energy balance error is defined as:

$$\Delta E_r = \frac{\sum_{k=1}^n E_k}{\text{MAX}(E_k)} \quad (10)$$

where  $n$  is the number of circuit elements including sources and  $\text{MAX}(E_k)$  gives the energy with the maximum module.

The time step is chosen computing  $\Delta E_r$  and the assumed time step is accepted if  $\Delta E_r \leq EER$ , where EER is the imposed relative energy balance error margin. The algorithm for the time step choice can be outlined as follows:

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 $t_{n+1} = t_n + h_n$ 
solve for  $t_{n+1}$ 
compute  $\Delta E_r$ 
if  $\Delta E_r < EER/10$ 
    accept  $t_{n+1}$ 
     $h_{n+1} = 2 \cdot h_n$ 
     $h_{n+1} = \min(h_{n+1}, TMAX)$ 
    continue
else if  $EER/10 < \Delta E_r < EER$ 
    accept  $t_{n+1}$ 
     $h_{n+1} = h_n$ 
    continue
else if  $\Delta E_r > EER$ 
    reject  $t_{n+1}$ 
     $h_{n+1} = h_n/2$ 
    if  $h_{n+1} < H \text{ min}$  print TIME STEP TOO SMALL; analysis is aborted

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The algorithm based on the relative energy balance error in a time step guarantees a relative energy balance error less than the imposed value EER on the whole time interval (from  $t_{start}$  to  $t_{stop}$ ). This is a global estimate of the correctness of the transient analysis for the whole circuit and for the whole time interval.

This algorithm has been implemented in C and has been tested on linear circuits with damped oscillatory responses.

### 3. EXAMPLE

The circuit in Fig. 1 has been analyzed starting from an initial condition chosen so that to give a damped oscillatory response ( $v_C = 2V$ ,  $v_{Cl} = 1V$ ,  $i_{Ll} = 0A$ ). This circuit is driven by a sinusoidal voltage of 1 V and 1 MHz. The voltage of the capacitor C is given in Fig. 2 for  $t_{stop} = 1\mu s$ .

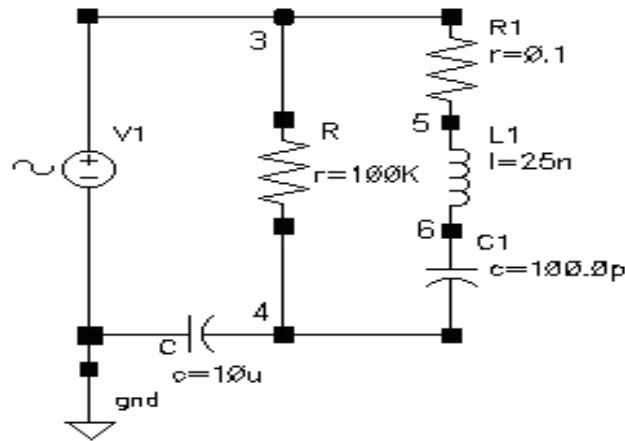


Fig. 1. Linear circuit with damped oscillatory response

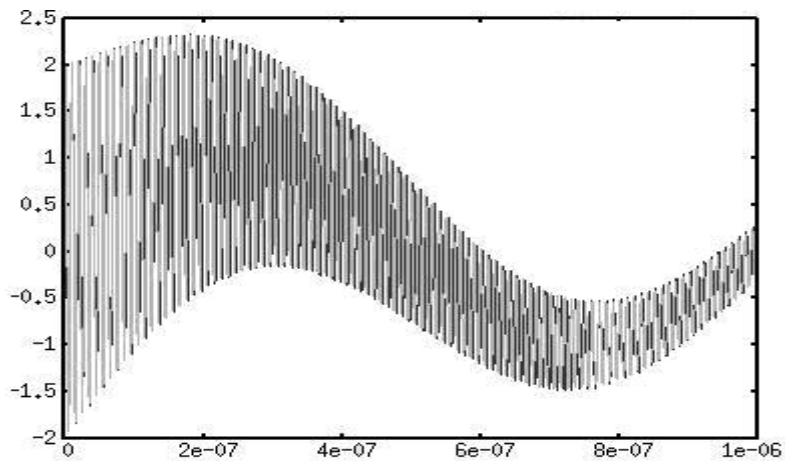


Fig. 2. The circuit response for  $t_{stop}=1\mu s$

In order to compare the results of SPICE and of the proposed algorithm, two cases were taken into account. The parameters of the PSPICE analysis and of the proposed algorithm are given in Table 1.

Table 1

Algorithm	Errors	Accepted steps	Rejected steps
SPICE	reltol=2e-3, abstol=1e-15	3869	1613
proposed	ERR=6e-3	3931	63

The error parameters of the analyses have been chosen so that the number of accepted time steps is nearly the same for both methods. The high frequency details are given in Fig. 3.

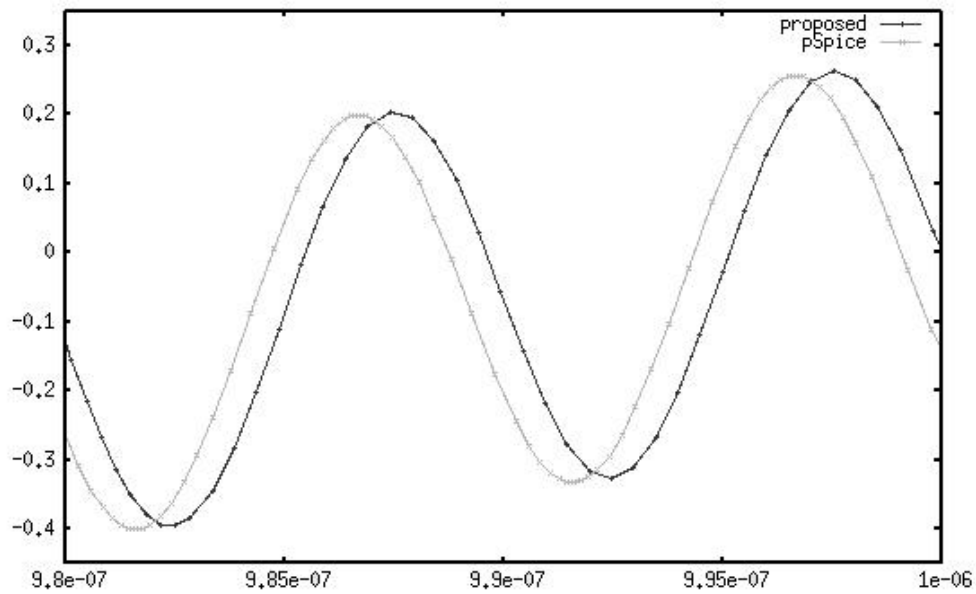


Fig. 3. The circuit response in the first case (high frequency detail)

The second case uses smaller error margins, the parameters of the analyses being given in Table 2. The circuit response is given in Fig. 4.

Table 2

Algorithm	Errors	Accepted steps	Rejected steps
SPICE	reltol=1e-6, abstol=1e-15	10688	2861
proposed	ERR=6e-5	10573	1758

In both first and second cases it can be observed that the proposed algorithm rejects fewer steps than the SPICE one, the number of accepted steps being similar. The similar number of accepted steps follows from the condition of similar accuracy which must be ensured in order to compare the two algorithms. In the second case, which uses smaller error values than the first one, the high frequency details given by SPICE and the proposed algorithm are closer each other than in the first case.

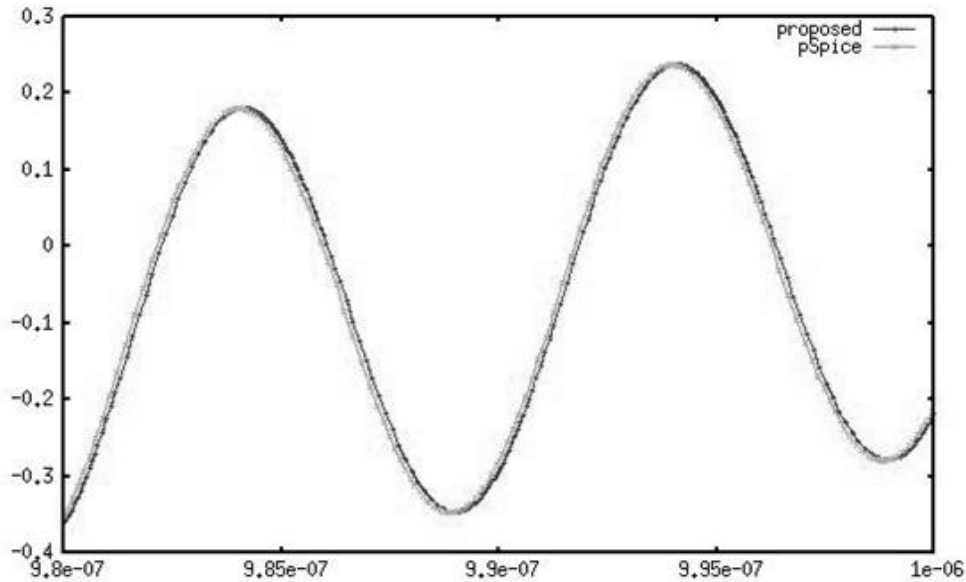


Fig. 4. The circuit response in the second case (high frequency detail)

#### 4. CONCLUSIONS

A new error for transient analysis of electrical circuits is proposed in this paper. A new algorithm for time step choice using this error has been developed. Some preliminary tests show that for a similar number of accepted steps (which leads to a similar form of the transient response), the proposed algorithm rejects fewer steps than the SPICE algorithm.

Future work will be devoted to comparison with analytical solutions, investigation of the “frequency warping” phenomenon in high Q circuits, and adaptive algorithms for time step choice.

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## REFERENCES

1. L. W. Nagel, *SPICE2: A computer program to simulate semiconductor circuits*, Memorandum No. UCB/ERL M520, University of California, Berkeley, 1975.
2. L. O. Chua, P. M. Lin, *Computer aided analysis of electronic circuits*, Prentice Hall, 1975.
3. A. Brambilla, D. A'Amore, *Energy-Based Control of Numerical Errors in Time-Domain Simulation of Dynamic Circuits*, IEEE Transactions on Circuits And Systems – I: Fundamental Theory And Applications, Vol. 48, No.5, May 2001.
4. <http://brambilla.elet.polimi.it>
5. A. Brambilla, *Private communication*, March 2007.
6. F. Constantinescu, A. G. Gheorghe, M. Nitescu, *Large signal analysis of RF circuits – an overview*, Proceedings of ATEE 2006.