

# STATIC CONDENSATION FOR ASPEEC MODELS BASED ON HIERARCHICAL MATRICES

Marius-Cristian Radulescu and Daniel Ioan

“Politehnica” University of Bucharest, Electrical Engineering Department, Numerical Methods Laboratory, [lmn@lmn.pub.ro](mailto:lmn@lmn.pub.ro)

**Abstract** – Due to the increase of the operation frequency and the down-scaling of the on-chip size, the parasitic effects of the electromagnetic field cannot be neglected any longer in the design of ICs. The high frequency field modeling of on-chip passive components and interconnects was one of the topics addressed by the FP5/IST/Codestar project ([www.imec.be/codestar](http://www.imec.be/codestar)). The reference method for the modeling of passive structures is considered to be PEEC, based on Green function. One of the main disadvantages of PEEC is that it requested Green function. Moreover the accurate modeling of the skin effect needs detailed discretization of conductors. Thus, the method is relatively expensive from the memory requirement point of view. An alternative approach for the electromagnetic field modeling is proposed in this paper. It is based on the Finite Integration Technique (FIT), which does not use Green functions and it generates a model having a number of degrees of freedom at least as small as PEEC.

## 1. PRELIMINARIES

The reference method for the modeling of passive structures is considered to be PEEC, based on Green function [2,3]. In this method, the conductors are discretized in filaments, in which constant current densities flow and their surfaces are discretized in panels having constant charge density. An equivalent RLC circuit containing a resistance for each filament, coupling inductances between whatever two filaments and capacitors between whatever two nodes can be conceived. The inductances and capacitances of such a circuit are described by full matrices. One of the main disadvantages of PEEC is that the accurate modeling of the skin effect needs detailed discretization of conductors. Thus, the method is relatively expensive from the memory requirement point of view. For instance, a 64 b bus with 10 segments per line and 6 filaments per segment conduces to  $n = 6 \times 10 \times 64 = 3840$  RL branches,  $n(n-1)/2 = 7,370,880$  couplings and  $11 \times 64 \times 12 = 495,616$  C branches, yielding a total number of 7,874,176 elements. Several acceleration techniques, such as fast multipole [4], SVD [5], hierarchical approach [6], FFT [7], etc., are proposed to manage this difficulty.

An alternative approach for the electromagnetic field modeling is proposed in this paper. It is based on the Finite Integration Technique (FIT), which does not use Green functions and which generates a model having a number of degrees of freedom at least as small as PEEC.

FIT is a numerical method able to solve field problems [8], based on spatial discretization "without shape functions". FIT starts from the global form of electromagnetic field equations. Its degrees of freedom (dofs) are not local field components, but the global variables i.e. voltages and fluxes assigned to grid elements (edges and faces, respectively). Two Yee type staggered grids are used as discretization mesh. They are usually orthogonal, but they can be non-orthogonal Delaunay/Veronoi meshes as well. The Maxwell Grid Equations (MGE) obtained by FIT are:

$$\mathbf{D} \cdot \mathbf{d} = \mathbf{q}, \mathbf{D}' \cdot \mathbf{b} = \mathbf{0}, \mathbf{C} \cdot \mathbf{e} = -\frac{d\mathbf{b}}{dt}, \mathbf{C}' \cdot \mathbf{h} = \mathbf{j} + \frac{d\mathbf{d}}{dt}, \quad (1)$$

where  $\mathbf{e}$  is the vector of emfs along the edges of the primary grid,  $\mathbf{d}$  is the vector of electric fluxes through the faces of the secondary grid,  $\mathbf{h}$  is the vector of mmfs along the edges of the secondary grid,  $\mathbf{b}$  is the vector of magnetic fluxes through the faces of the primary grid,  $\mathbf{j}$  is the vector of currents through the faces of the secondary grid,  $\mathbf{q}$  is the vector of charges in the secondary grid cells. The  $\mathbf{D}$  operator is the discrete divergence and the  $\mathbf{C}$  operator is the discrete curl. The ' notation refers to the secondary grid.

One important feature of FIT is that there are no discretization errors in the fundamental (metric-free) MGE. The equations are sparse, mimetic and conservative. Due to this, no spurious modes arise in the numerical solution.

The material behavior is described by means of the Hodge's operators:

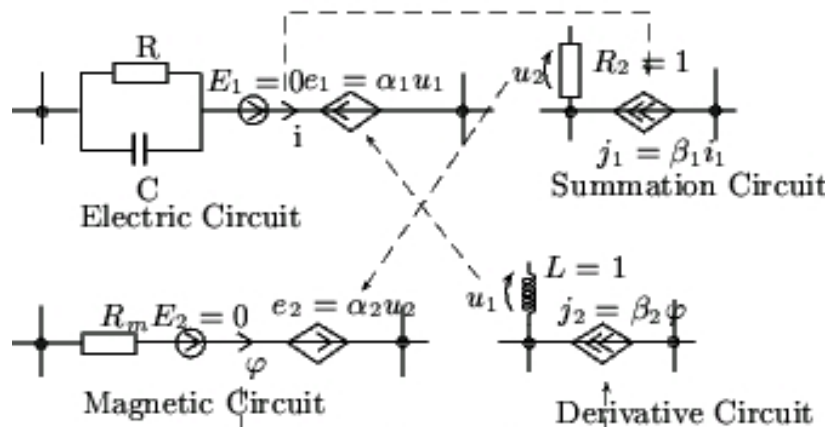
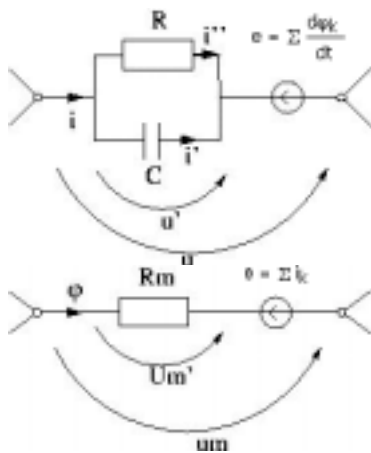
$$\mathbf{d} = \mathbf{M}_\epsilon \mathbf{e}, \mathbf{b} = \mathbf{M}_\mu \mathbf{h}, \mathbf{j} = \mathbf{M}_\sigma \mathbf{e} \quad (2)$$

These constitutive equations are metric-dependent and they hold the discretization error.

The ASPEEC technique detailed in this paper is part of the ALLROM strategy [9], developed by LMN team within the CODESTAR project.

### MAGNETO-ELECTRIC EQUIVALENT CIRCUITS (MEEC)

From (1) and (2), an equivalent circuit can be derived (actually two mutual coupled circuits, as in **fig. 1**)[17].



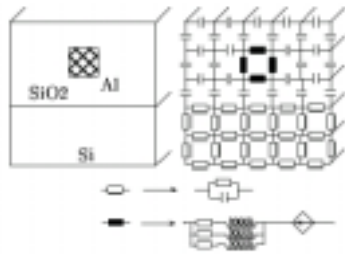
**Fig. 1:** Typical branches of electric (top) and magnetic (bottom) circuits.

**Fig. 2:** Typical branches of the four SPICE-like subcircuits: electric, magnetic, summation, derivative.

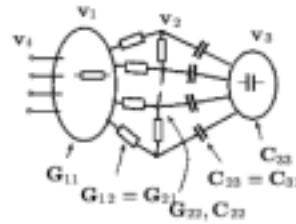
The SPICE equivalent circuit for the full-wave distributed model consists of four mutual coupled sub-circuits: electric, magnetic, summation and derivative circuits (**fig. 2**).

The SPICE equivalent circuit thus derived has linear complexity (nodes and branches number versus the number of FIT grid cells), while the PEEC model has a quadratic complexity due to their full RL matrices. However, the number of dofs is still large, as comparing to PEEC based on Electro-Magneto-Quasi-Static field. In order to reduce the number of dofs associated to the *MEEC* model, the conductive domains (metal and poly-silicon) are modeled with magneto-quasi-static field (MQS) with frequency dependent Hodge operators [10]. In this way, the grid on the cross section does not need to be refined in order to take into account the frequency effect. In this case, the equivalent electric circuit has no parallel capacitances, but three series RL cells with non-coupled inductances replacing  $R$  and  $R_m$  [10]. The sub-domains

with low conductivity (e.g. low doped Si) can be modeled with electro-quasi-static field (EQS) superposed with magneto-static field. Both induced emf and total current are vanished. Resistance in the electric circuit can be also disregarded in order to model insulating domains (e.g. SiO2 and low k).



**Fig. 3:** Example of distributed circuit equivalent to EMQS model



**Fig. 4:** The distributed circuit, with RC separated parts

The obtained EMQS model (**fig. 3**) is smaller than the Full Wave model, but still larger than PEEC due to the nodes in the insulator sub-domain.

### ALGEBRAIC REDUCTION OF PARTIAL ELECTRO-MAGNETIC EQUIVALENT CIRCUIT (APEEC)

To reduce the model size to that of PEEC's, the generalized delta-star transforms of capacitors and magnetic reluctances in EMQS-MEEC can be carry out. In this way, all internal electric nodes in insulators and internal magnetic nodes in non-conductors are removed. (**fig. 4**). This static condensation procedure eliminates nodes that are non-essential, i.e. nodes having no state variables associated to them. The equivalent reduced circuits obtained (we call them *APEEC*) are similar to those obtained by the VPEC technique based on integral equations of EMQS field [11]. Each node elimination in APEEC is equivalent to one step of algebraic Gauss-elimination. After the elimination of a node, a fill-in appears in the matrix involved. The fill-in depends very much of the elimination order. In order to preserve the matrix symmetry, only diagonal permutations (equivalent to node re-ordering) are allowed. To find optimal re-ordering (minimal fill-in) a problem with NP complexity should be solved. Therefore, only heuristic techniques to find pseudo-optimal ordering can be used (e.g. the Marcowitz technique). After algebraic reduction, the capacitors and magnetic reluctances in APEEC are described by full  $\mathbf{C}$  and  $\mathbf{G}_m$  matrices, which are the Schur complements of the initial sparse nodal matrices. Let us take for instance the simple electro-quasi-static case, and assume that the distributed RC circuit obtained by discretization has the resistive part separated from the capacitive one (**fig. 4**).

This case, often encountered in practical devices incorporating metals and dielectrics, is described by a system of differential algebraic equations:  $\mathbf{C} \frac{d\mathbf{v}}{dt} = -\mathbf{G}\mathbf{v} + \mathbf{S}\mathbf{i}_t$ , where both nodal capacitances  $\mathbf{C}$  and nodal conductances  $\mathbf{G}$  are singular matrices, and the terminal voltages are:  $\mathbf{v}_t = \mathbf{S}_1^T \mathbf{v}_1 + \mathbf{S}_2^T \mathbf{v}_2$ .

Partitioning the semi-state space vector in  $\mathbf{v} = [\mathbf{v}_1, \mathbf{v}_2, \mathbf{v}_3]^T$  as in (**fig. 4**), the following sub-matrices will be null:  $C_{11}, C_{12} = C_{21}, C_{13}=C_{31}, G_{33}, G_{13}=G_{31}, G_{23}=G_{32}$ . Therefore, the following state-space equations can be derived as:

$$(\mathbf{C}_{22} - \mathbf{C}_{23}\mathbf{C}_{33}^{-1}\mathbf{C}_{32}) \frac{d\mathbf{v}_2}{dt} = -(\mathbf{G}_{22} - \mathbf{G}_{21}\mathbf{G}_{11}^{-1}\mathbf{G}_{12})\mathbf{v}_2 - \mathbf{G}_{21}\mathbf{G}_{11}^{-1}\mathbf{S}_1\mathbf{i}_t + \mathbf{S}_2\mathbf{i}_t \quad (6)$$

$$\mathbf{v}_t = (\mathbf{S}_2^T - \mathbf{S}_1^T \mathbf{G}_{11}^{-1} \mathbf{G}_{12}) \mathbf{v}_2 + \mathbf{S}_1^T \mathbf{G}_{11}^{-1} \mathbf{S}_1 \mathbf{i}_t.$$

This is the proof that, in the case of EQS field in conductor and dielectric structures (each cell is either a perfect insulator or a conductor), the state variables are the potentials of the nodes placed on the conductor-dielectric interfaces ( $\mathbf{v}_2$ ). The state equations of this minimal model are obtained by computing the Schur complements of the matrices  $\mathbf{C}_{11}$  (nodal capacitances of the dielectric part) and  $\mathbf{G}_{11}$  (nodal conductances of the conductive part). In order to compute the Schur complement, the LU factorization algorithm (e.g. MUMPS [12] sparse implementation) is applied to the  $\mathbf{C}$  and  $\mathbf{G}$  matrices. If this algorithm is interrupted after the internal node elimination, then the not-yet-factorized block is exactly the desired Schur complement.

### SPARSEFICATION OF ALGEBRAIC PEEC

The nodal capacitance matrix  $\mathbf{C}$  that describes the capacitive part of APEEC is a full, symmetric, positive definite, diagonal dominant, M-matrix (the diagonal has positive elements and off diagonal elements are negative). The nodal magnetic susceptance matrix  $\mathbf{G}_m$  ( $G_{mij} = -1/R_{mij}$ ) which describes the inductive part of *MEEC* has similar properties as  $\mathbf{C}$ , and therefore it can be sparsified using similar techniques. It is similar to K - element method used to describe coupled inductors [13], having their advantages.

The problem of sparsefication is to find sparse approximations of the matrices  $\mathbf{C}$  or  $\mathbf{G}_m$  (or a representation by a sparse matrix, such as SVD truncation), which keep their proprieties (e.g. if passivity is preserved, it is called *passivity-guaranteed sparsefication*).

It would be ideal if circuit representations will be kept after sparsefication (if capacitive/resistive equivalent circuit having lower number of elements can be synthesized, it is called *realizable sparsefication*).

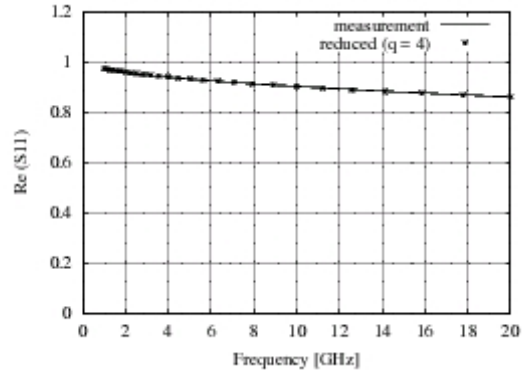
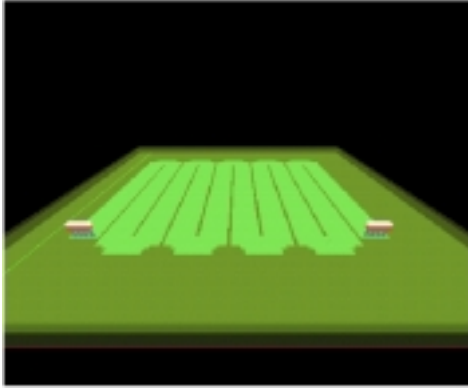
Two kinds of sparsefication are known. The *geometric sparsefication* is based on the observation that close interactions are stronger than far interactions, and therefore the former should be accurately described. In this type of sparsefication, the "distance" between nodes plays an important role. In *numeric sparsefication*, the neglectable elements of the matrices are dropped-off. In both matrices, any neglectable non-diagonal element and its symmetric can be vanished without losing the desired properties. The preferable criterion to detect if an element is neglectable or not, is to compare its value with the corresponding diagonal element.

Any acceleration method encountered in the numerical solving of the electromagnetic field integral equations can be considered as a sparsefication technique. However, we prefer a simpler but effective technique called hierarchical geometric sparsefication (HGS), followed by a numeric sparsefication. The idea behind HGS is to use fine grids for close interactions and coarse grids for far interactions, as in the hierarchical matrices (Hlib) approach [14]. For  $n$  nodes, the number of non-zero elements after sparsefication is of the order  $O(n \log n)$ .

The ASPEEC (Algebraic Sparsefied Partial Equivalent Element Circuit) model generated by the sparsefication of the APEEC model can be further reduced, using Krylov ROM techniques [15] or by circuit transform such as TICER [16], as posteriori ROM.

### NUMERICAL RESULTS

This section holds numerical results related to the application of ASPEEC technique to one of Codestar benchmark, the meander resistor (**fig. 5**).



**Fig. 5:** Codestar meander resistor benchmark – **Fig. 6:** Real part of S11 versus frequency. RPOLY2\_ME.

The computational domain has the dimensions (in  $\mu\text{m}$ )  $48 \times 43.5 \times 2.937$ , discretized with an initial mesh having 368,200 nodes, which corresponds to 2,209,680 dofs. A macromodel with 5,940 nodes (19,510 dofs) was extracted by the ALLROM strategy. After applying the ASPEEC technique, the number of dofs decreased to 1,882. The evaluation of the frequency characteristics was carried out in accordance with an adaptive frequency sampling technique in 11 points. The final model order, obtained at the end of the a posteriori ROM was  $q=4$ . The whole ALLROM computing time on a standard PC is 145 s, and the relative error  $\varepsilon = \text{rms} \|\mathbf{S}_{\text{ref}} - \mathbf{S}\|_F / \max_f \|\mathbf{S}_{\text{ref}}\|_F$  between the measurement and the simulation being 1.4% (**fig. 6**). In the error computation, the Frobenius norm is used,  $\mathbf{S}_{\text{ref}}$  are the reference scattering parameters, and the maximum is computed with respect to the frequency range of interest (e.g.  $0 < f < 20$  GHz in our case).

## CONCLUSIONS

The paper presents a powerful technique to extract reduced order models of on-chip passive structures, included in a new compact modeling technology. The distributed equivalent circuit we propose has a linear complexity, it is similar to VPEC, but is based on FIT, not on the integral approach (PEEC). Using algebraic techniques (Schur complement), APEEC method reduces the FIT equations (and the associated equivalent circuit) to ones similar to PEEC (having the same number of dofs). To be effective in simulation, the APEEC matrices are approximated by sparse ones, conducting to the ASPEEC model. The proposed approach combines advantages of FIT with those of PEEC, providing:

- more flexibility in the modeling of conductor/insulator/substrate non-homogeneous structures;
- Green functions are not required;
- accurate models for skin effects, without significant increase of computational effort;
- fast and accurate direct SPICE equivalent circuits with low complexity for any full-wave, EMQS, MQS or EQS model;
- when applying the proposed method, the explicit build of equivalent circuits is not a compulsory step; they can be used as software objects in order to represent the model of the device or for checking purposes (however, its theoretical importance is without any doubt);
- structural passivity preservation;
- same (realizable and passivity guaranteed) sparsefication technique is applied for both capacitance and inductance components of the extracted model.

The proposed approach proved to be suitable for the Codestar benchmarks most of them being simulated with accuracy better than 5 %.

**ATEE - 2004**  
**REFERENCES**

- [1] Codestar Website, "<http://www.imec.be/codestar>".
- [2] P.J. Restle, A.E. Ruehli, S.G. Walker, and G. Papadopoulos, "Full-wave PEEC time-domain method for the modeling of on-chip interconnects" IEEE Trans. on CAD of Integrated Circuits and Systems, vol. 20, no. 7, pp. 877--86, 2001.
- [3] A.M. Niknejad, R. Gharpurey, and R.G. Meyer, "Numerically Stable Green Function for Modeling and Analysis of Substrate Coupling in Integrated Circuits", IEEE Trans. on CAD of Integrated Circuits and Systems, vol. 17, no. 4, pp. 305--315, 1998.
- [4] K. Nabors and J. White, "FastCap: A multipole-accelerated 3-d capacitance extraction program", IEEE Trans. CAD, vol. 10, pp. 1447--1459, 1991.
- [5] S. Kapur and D.E. Long, "IES3: a fast integral equation solver for efficient 3-dimensional extraction", in Int. Conf. on CAD, 1997, pp. 448--455.
- [6] Weiping Shi, Jianguo Liu, Naveen Kakani, and Tiejun Yu, "A fast hierarchical algorithm for three-dimensional capacitance extraction", IEEE Transactions on CAD of Integrated Circuits and Systems, vol. 21, no. 3, 2002.
- [7] Zhenhai Zhu, Ben Song, and Jacob White, "Algorithms in fastimp: A fast and wideband impedance extraction program for complicated 3d geometries", in IEEE/ACM DAC, Anaheim, CA, USA, 2003.
- [8] M. Clemens and T. Weiland, "Discrete Electromagnetism with the Finite Integration Technique", Progress In Electromagnetics Research, PIER, vol. 32, pp. 65--87, 2001.
- [9] D. Ioan, G. Ciuprina, M. Radulescu, and M. Piper, "All levels models strategy to reduce the model order of on-chip passive components", in IEEE Conf. on Electromagnetic Field Computation CEFC 2004, Digest Book, Seoul, Korea, 2004.
- [10] D. Ioan, and M. Piper, "Fit models with frequency dependent hodge operators for hf effects in metallic conductors", in PIERS, Pisa, Italy, 2004.
- [11] Hao Yu and Lei He, "Vector potential equivalent circuit based on peec inversion" in 40th ACM/IEEE DAC, Anaheim, CA, USA, 2003, pp. 718--723.
- [12] A. Guermouche, J.Y. L'Excellent, and G. Utard, "Impact of reordering on the memory of a multifrontal solver", Parallel Computing, Report RR2003-08/INRIA/RR-4729, vol. 29, pp. 1191--1218, 2003.
- [13] A. Devgan, H. Ji, and W. Dai, "How to efficiently capture on-chip inductance effects: Introducing a new circuit element k", in IEEE/ACM Int. Conf. on CAD, 2000, pp. 150--155.
- [14] Wolfgang Hackbusch, "A sparse matrix arithmetic based on h-matrices", Computing, vol. 62, pp. 89--108, 1999.
- [15] Mustafa Celik, Lawrence Pileggi, and Altan Odabasioglu, "IC Interconnect Analysis", Kluwer Academic Publishers, 2002.
- [16] Bernard N. Sheehan, "Ticer: realizable reduction of extracted rc circuits", in IEEE/ACM Int. Conf. on CAD, San Jose, California, 1999, pp. 200--203.
- [17] Daniel Ioan, Gabriela Ciuprina and Marius Radulescu, "Algebraic Sparsified Partial Equivalent Electric Circuit (ASPEEC)", SCEE 2004, Capo d'Orlando, Italy.