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CODESTAR BENCHMARK STRUCTURES: COMPARISON BETWEEN MEASUREMENTS AND SIMULATIONS

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Abstract**:** *The paper describes the benchmarks used within the FP5/IST/Codestar European project dedicated to compact modeling of on-chip structures at high frequency. These benchmarks are test structures aiming to validate the developed CAD software dedicated to compact model extraction. They play an essential role in the project, because its success is measured by the matching between simulation and measured results for these benchmarks.*

1. INTRODUCTION

In integrated circuit technology, cost aspects drive the need for incorporating passive components on-chip, and downscaling of the chip dimensions. Due to the closer distance between conductors and the increase of operating frequency, parasitic electromagnetic field effects are a potential cause for erroneous design. In order to decrease the design time and to avoid unnecessary extra mask sets, understanding and quantifying of parasitic effects is necessary before manufacturing. This can be achieved by computer simulation.

The modeling of passive on-chip components and interconnects was the target of the FP5/IST/Codestar European project (www.imec.be/codestar) [1]. The path from the layout and technological information to a compact model described as a net list is not an easy one, considering the problem complexity. Our approach is based on a strategy called ALLROM, aiming to reduce the complexity of the problem, i.e. the number of degrees of freedom (dofs) at all stages/levels of the simulation process. This strategy is described in [2,3] and details can be found in [4,5].

In order to assess the quality of the electromagnetic simulation, dedicated test structures were designed, fabricated and characterized in the framework of the Codestar project, by two industrial partners: *Austriamicrosystems* (A) and *the Institute for microelectronics* (IMEC,B). The test-structures were measured and de-embedded, by these partners with advanced high frequency S-parameter measurement techniques. The simulations of test structures were made mainly by the academic partners, authors of CAD software. The comparison between measurements and simulations were carried out to assess the quality of the Codestar teamwork. In this paper, comparisons between measurements and simulation results obtained with software developed at Politehnica Univ. of Bucharest, Numerical methods Laboratory (LMN), based on FIT (Finite Integrals Techniques) are carried out

2. CODESTAR BENCHMARKS

To test the accuracy of the developed software, several benchmark devices aiming to model passive on-chip components and interconnects were chosen [6,7]. They can be grouped in four categories: resistors, capacitors, inductors, and transmission lines of various shapes and material properties. There are 32 benchmarks studied: two types of resistors (RPOLY): a meander one and a segmented one; two types of capacitors: poly-silicon (CPOLY) and metal-insulator-metal (CMIM) and three types of inductors: large, (SP-LARGE), middle (SP-MIDDLE) and small (SP-SMALL) sizes. A series of micro-strip and coplanar transmission lines, representing different technologies interconnects: Al/SiO2, Cu,/SiO2, Al/Lowk and

Cu/Lowk are studied as well. Challenging structures such as series LC cells, RF pads etc. are also proposed.

This paper shows the quantitative correlation between measurements and simulation for four typical Codestar benchmarks: a meander resistor, a metal insulator metal capacitor, a small spiral, a coplanar line and a spiral-capacitor cell.

High frequency measurement results have been provided in terms of S-Parameters and Line parameters (RLCG per unit length) after de-embedding.The Multiline-TRL (Thru-line-reflect) procedure is used to de-embed the measured s-parameters of the transmission line test structures. The M-TRL algorithm is one the most accurate VNA calibration procedure for on-wafer measurements and the basis of industry standard calibration software NIST Multical. The TRL procedure employs multiple lengths for a particular transmission line configuration and a separate reflect standard to accurately de-embed the DUT (Device under test) by eliminating the effect of contact-pad parasitics.

The accuracy and repeatability of high frequency measurements with the network analyzer is a critical aspect which has been verified by measuring the same structures both in IMEC and AMS; very good consistency in the results has been obtained.

There have been issues with the Cu-Oxide and Cu-Lowk structures. Cu-Lowk structures suffer from excessive attenuation at high frequency. This is due to the non-optimal insulator stack in terms of too low thickness, which causes a high resistance of the line. Long lines suffer from excessive attenuation, thus limiting the measurements accuracy; short lines have very high parasitic capacitance of the pads, much larger than the capacitance to be measured on the line thus making the de-embedding unfeasible. In both cases, the full set of RLCG parameters cannot be extracted; only the R and C parameters have been obtained. S-parameters without de-embedding are provided to make a comparison between measurements and simulations even without RLCG parameters available.

The Cu-Lowk architectures are forecasted as the most promising solutions to progress in the sub-100 nm node. In parallel, the less ambitious route consisting of Cu and Oxide is explored, since the lowk material remains critical with respect to mechanical stability. Also, a new Cu-Lowk run with optimized stack is foreseen. Therefore, IMEC provided test structures results to the full collection of the Codestar benchmark database.

The simulation data has required high frequency measurements on submicron technology structures for the extraction of tangent loss data, a parameter not available in the ITRS Roadmap. The results from Codestar simulations of these models allow to make predictions on the high frequency performance of future interconnect.

The challenging structures have been proposed as optional elements for the examination of some special effects requested by the end users. Some of them may be outside of the scope of. The challenging structures are all strongly relying on physical phenomena taking place in the substrate.

Every chapter concludes with the relative error value between the measurements and the results obtained from the simulated model. The value of the relative error is computed using relation (1).

$$er = \frac{rms\left\| S - S_{ref} \right\|_F}{max\left\| S_{ref} \right\|_F} \quad (1)$$

3. THE MEANDER RESISTOR BENCHMARK

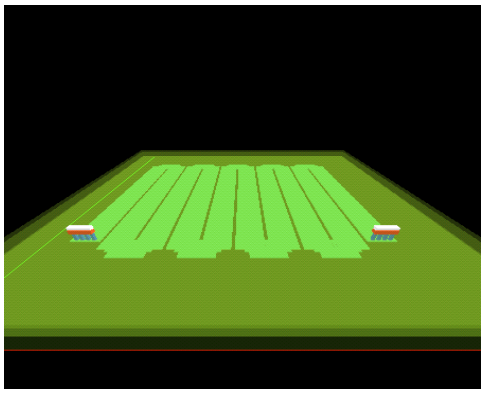

Fig.1: Meander resistor layout

The RPOLY benchmark (fig.1) has the following characteristics: the computational domain is 48µm ×43.5µm×2.937µm, the initial mesh has 368200 nodes, the frequency range is between 1GHz and 20GHZ, and it is current excited. The field models have about 2209680 degrees of freedom. A very good agreement between the simulated S parameters and the measurements has been obtained. The reduction was carried out using the vector fitting procedure and a reduced model of order 4 was obtained. The rms relative error between the measurements and the SPICE simulation of the final reduced compact model is 1.4 % (fig. 2).

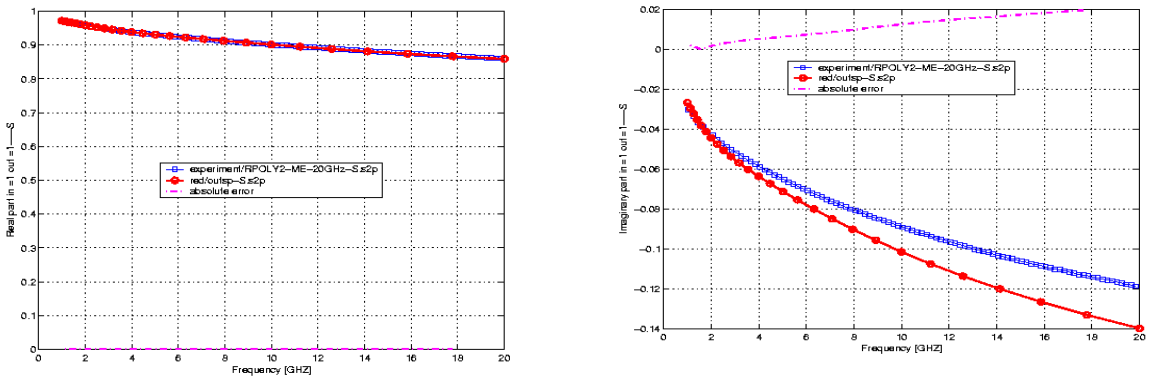

Fig.2: RPOLY_ME - Comparison between measurements and SPICE simulation of the reduced compact model – real (left) and imaginary (right) parts of the scattering parameter S11.

4. CMIM CAPACITOR BENCHMARK

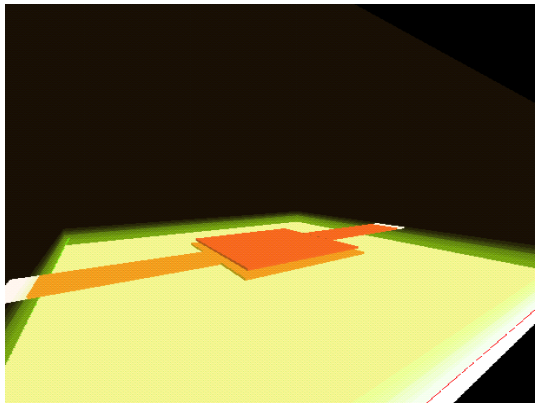

Fig.3: CMIM capacitor layout

The CMIM capacitor (fig.3) consists of an upper plate metal, a lower metal plate and an insulator. The computational domain is 89.95µm×89.95µm× 36.814µm. The CMIM capacitor has been simulated with the dFIT solver. The initial model has about 5000000 dofs. The obtained frequency response was used to generate a reduced model of order 4. Its

synthesized circuit was simulated with SPICE. A very good agreement between the simulated S parameter and the measurements has been obtained. The rms relative error between the measurements and the SPICE simulation of the reduced model is 2.5 % (fig.4).

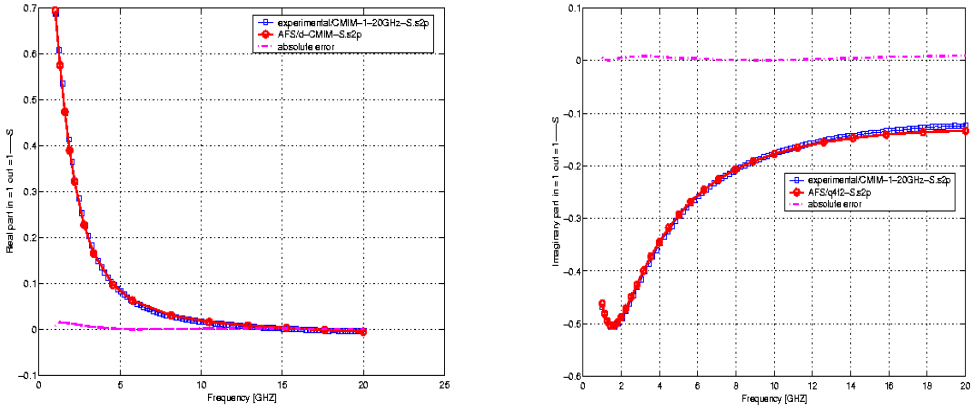

Fig. 4: CMIM - Comparison between measurements and SPICE simulation of the reduced compact model – real (left) and imaginary (right) parts of the scattering parameter S11

5. SMALL SPIRAL INDUCTOR BENCHMARK

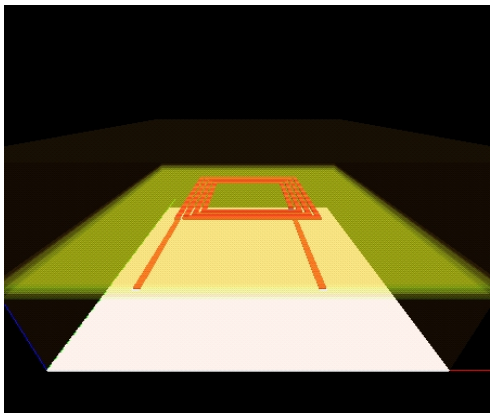

Fig.5: SP_SMALL layout

The SP_SMALL benchmark presented is a spiral inductor (fig.5). The computational domain is 330.45µm × 340.15µm × 5.617µm and the initial mesh has about 600000 nodes. The model has been simulated by DFIT and the rms relative error of the scattering parameters is 20%, but this is within the geometrical parameter tolerance given for this benchmark.

The model has been successfully reduced to order 4. The reduced model has been synthesized and the obtained sub-circuit was simulated with SPICE. The reduction and the synthesis are very accurate because the errors between the results from the SPICE simulation and the measurements are almost equal to the errors between the simulations and the measurements (fig.6).

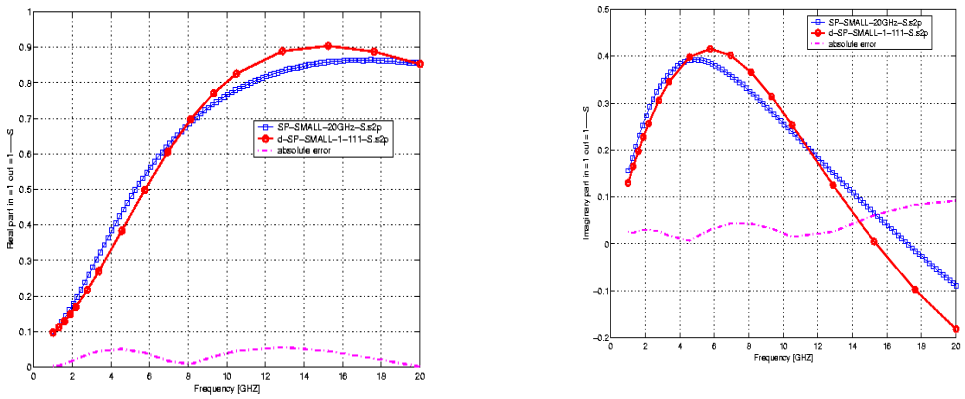

Fig. 6: CMIM - Comparison between measurements and SPICE simulation of the reduced model– real (left) and imaginary (right) parts of the scattering parameter S11

6. COPLANAR LINE AL/SIO2 BENCHMARK

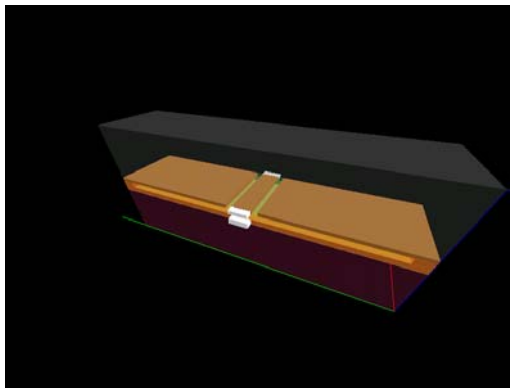

Fig. 7: Coplanar line layout

A metal line (conductivity $3.3e7\Omega^{-1}m^{-1}$, thickness 0.69μm and width 3μm) is separated from two metal planes (conductivity $3.3e7\Omega^{-1}m^{-1}$, thickness 0.69μm) with a layer of air (fig.7). Under this structure there is an oxide layer and again a metal plane of 1μm thickness. The reduced computational domain is 200μm × 46.588μm × 17.74μm. The model was simulated with DFIT solver and the results have been compared with the measurements.

The obtained frequency characteristics were used to derive a reduced model of order 10, using vector-fitting procedure. The reduced model was synthesized and the sub-circuit obtained was simulated with SPICE.

The rms relative error of the scattering parameters is less then 4.79 %.The errors between the results from the SPICE simulation and the measurements are almost equal to the errors between the results from DFIT simulation and the measurements (fig.8).

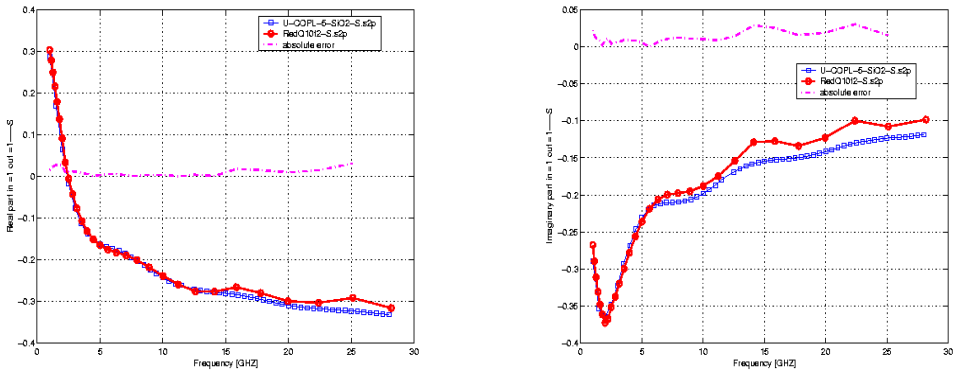

Fig. 8: Coplanar line - Comparison between measurements and SPICE simulation of the reduced model– real (left) and imaginary (right) parts of the scattering parameter S11

7. SPIRAL-CAPACITOR BENCHMARK

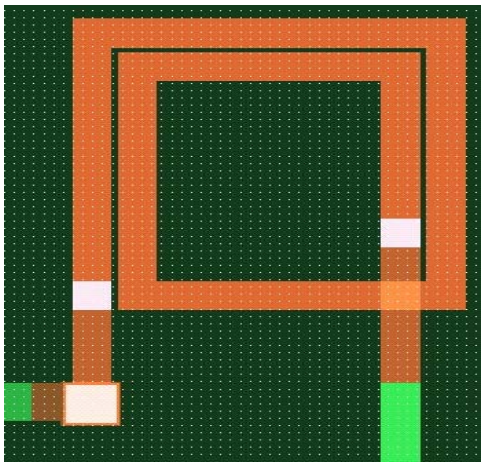

Fig. 9: Spiral-CMIM layout

The Spiral-CMIM (fig. 9) benchmark is a complex structure that is formed by a middle spiral and a metal-insulator-metal capacitor. The spiral structure was reduced to order 4 and synthesized with DEM and the capacitor structure was reduced with vector-fitting procedure to order 4 and than synthesized with DEM. After that both sub-circuits were chained and the obtained composed circuit was simulated with SPICE. The rms relative error between experimental results and the results obtained on a frequency range of 1-20GHz is less then 20% (fig. 10).

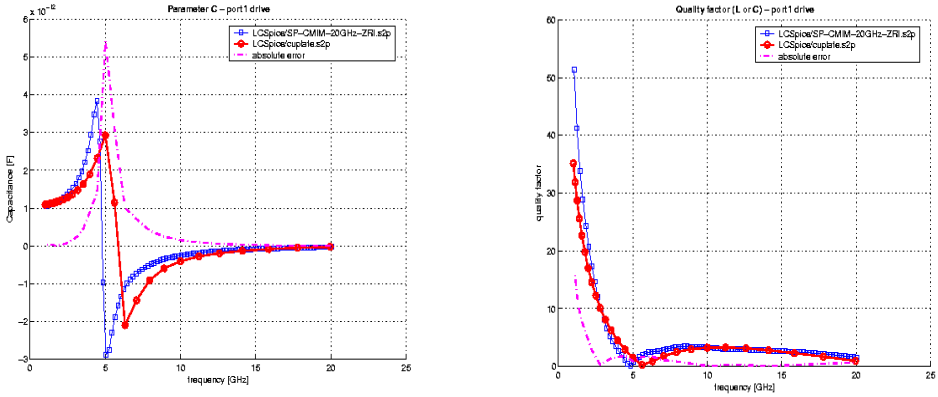

Fig. 10: SP-CMIM- Comparison between measurements and SPICE simulation of the reduced model – parameter C (left) and quality factor (right) on potr 1

7. CONCLUSIONS

The main goal of the CODESTAR project was the development of a code dedicated for the electromagnetic simulation of passive on-chip structure resulting in a small simulation network. Considering the large amount activities as well as the large variety of benchmarks, the project has reached a major part of its goals. Starting from the layout description, the result of the CODESTAR code is an equivalent net list of passive elements and interconnected patterns taking into account the detailed electrodynamics of passive on-chip structures, that can be loaded into a compact model simulator (SPICE).

A solver available with the CODESTAR software is based on an original method, the Dual Finite Integration Technique (dFIT). It has proven to be a very robust method to achieve acceptable results in a reduced simulation time.

Dedicated structure to test high-frequency simulations and compact models are described. These test structures were measured and simulated. Based upon the simulations compact (SPICE) models are constructed. A very good agreement between the compact model and measurements has been obtained (less than 5 % or within the technological spread and measurement errors).

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