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THE OBJECTIVES AN SCIENTIFIC ACHIEVEMENTS OF THE EUROPEAN RESEARCH PROJECT FP5/IST/CODESTAR

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Abstract The paper presents the main scientific objectives and achievements of the FP5/IST European research project entitled *"CODESTAR - Compact modeling of on-chip passive structures at high frequencies"*. The main goal of the CODESTAR project is the development of a code dedicated to the electromagnetic modeling and simulation of passive on-chip structures. First a detailed analysis of the test structure is carried out using an electromagnetic field solver. The outcome of the field solver is a full net list describing the detailed characteristics of the passive structure. This net list will be too large to be useful and therefore a systematic reduction of the net list must be done (i.e. reduced-order modeling). The resulting compact equivalent lumped-element model is inserted back into the full design scheme and the design cycle can be pursued. Parallel fabrication, characterization and evaluation of dedicated test structures is carried out, in order to validate the CODESTAR-code. The matching between experimental and CODESTAR simulation results is the measure of the project success.

1. INTRODUCTION

With the further downscaling of the IC technology, the operational frequencies of the signals are in the Giga Hertz range. As a consequence, the use of lumped-element parameters for the simulation or emulation of IC designs is too crude to generate reliable lay-outs. The reason is that the lumped element parameters are obtained in the static regime and these parameters ignore many effects that become pronounced in at high frequencies. In other words: interconnects and integrated passives behave qualitatively different at high frequencies as they do at low frequencies. Another major concern for on-chip design is that the high frequency characteristics or electromagnetic behavior is very sensitive to the material properties of the environment. In practice this means that if one designs a runner or passive component, its properties will alter dramatically, if the same runner or integrated passive component is placed above a semiconducting substrate and surrounded by dielectric material layers. These issues have been identified as a potential show stopper for robust designing deep submicron IC layouts and to optimally designing integrated passive components on chip. Furthermore, the increasing desire to put systems on a chip (SOC) demands good control over undesirable interferences. The latter usually pop up at higher frequencies. In particular, parasitic coupling through the substrate will hamper a successful implementation of system on a chip.

The fact that high frequency issues can no longer be ignored in IC design has urged the contributors to the International Technology Roadmap for Semiconductors (ITRS, www.itrs.org) to declare the high-frequency modelling (> 5 GHz) as a *grand challenge* that should be solved in order to continue the pace of progress that was witnessed in the last three decades.

To accelerate the design of on-chip structures and interconnects the development of new modeling algorithms is needed. This task was addressed by an European joint research project entitled *"CODESTAR - Compact modeling of on-chip passive structures at high frequencies"* and

carried out within Fifth Framework Program, the thematic component Information Society Technologies (IST).

The project was defined by following three leading principles acting in the background:

· In order to capture the high-frequency effects, the full physics of electromagnetism needs to be considered. In particular, this means that no restrictive assumptions are implemented a priori.

· Experimental data need to be produced in order to guarantee that the solutions that are generated within CODESTAR have practical value and the methods can be used in an industrial environment.

· Computation times should be in an acceptable range. Considering the complexity of the problem this will lead to a trade-off between speed, accuracy and predictability.

2. OBJECTIVES OF THE PROJECT

The main goal of the CODESTAR project is the development of a code dedicated for the electromagnetic simulation of passive on-chip structures resulting in a small simulation network. First a detailed analysis of the test structure is carried out using an electromagnetic field solver. The outcome of the field solver is a full net list describing the detailed characteristics of the passive structure. This net list will be too large to be useful and therefore a systematic reduction of the net list must be done (i.e. reduced-order modeling). The resulting compact equivalent lumped-element model is inserted back into the full design scheme and the design cycle can be pursued. Parallel fabrication, characterization and evaluation of dedicated test structures is carried out, in order to validate the CODESTAR-code. The matching between experimental and CODESTAR simulation results is the measure of the project success.

The project is sub-divided in five major building blocks (work-packages), as indicated in figure 1. Two of them, i.e. the MAXWELL SOLVERS part and REDUCED-ORDER MODELING part have a strong interdisciplinary research character. These parts apply the first guiding principle, i.e. that no unjustified simplifications are allowed (faithful physical modeling) IMPLEMENTATION is the realization into operational software, while TEST STRUCTURES deals with the input from users (industries) and the characterization of the results. Finally, EXPLOITATION and DISSEMINATION has resulted into a valid business model of the produced code.

3. CODESTAR PROJECT: DATA AND FACTS

Title of the project: Compact models of on-chip passive structures at high frequency

Project code: CODESTAR– IST- 2001- 34058

Duration of the project: The Codestar project started March 1, 2002 and will run for 30 months until the end of August 2004. The total effort within CODESTAR amounts to 241 person*month .

Partners of the project:

- Partners from industry:
  - IMEC (MAGWEL) - Belgium (www.imec.be, www.magwel.com)
  - AustriaMicroSystems (AMS) - Austria (www.austriamicrosystem.com)
  - Philips - Netherland (www.philips.nl)
- Academic Partners:
  - Technical Univ. Eindhoven - TU/e - Netherland (www.tue.nl)
  - Univ. of Gent - RUG - Belgium (www.rug.ac.be)

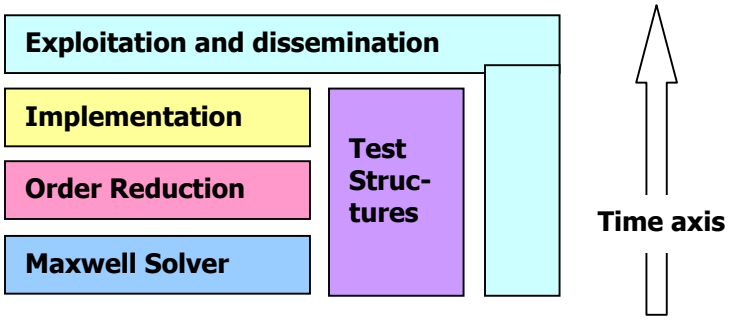

Fig. 1. Codestar Worck Packages

MAGWEL (Belgium) spin-off company that was a direct result of the CODESTAR project. Its s goal is to make the results that have been produced within CODESTAR (and related work) available to the semiconductor industry.

4. FIELD SOLVERS

The following solvers have been selected for an in-depth study and for being applied to on-chip integrated passives and interconnect:

- **The Lattice-Gauge Solver (LG)** by MAGWEL**;**
- **The Finite-Integrals Technique Solver (FIT)** by LMN;
- **The Finite-Difference Time Domain Solver (FDTD)** by RUG;
- **The Partial-Equivalent Electric Circuit Solver (PEEC)** by TU/e.

The Lattice-Gauge Solver exploits ideas that were originally developed in Quantum Chromodynamics. The solver is new in its formulation of the electromagnetic field problem. The LG solver uses as fundamental degrees of freedom, the electromagnetic scalar potential and the vector potential. The gauge condition is respected in the Coulomb gauge and ghost field degrees of freedom were added in order to create a well-defined mathematical problem. The lattice gauge solver has been selected because it has a direct connection with the Technology Computer-Aided Design (TCAD) methods that are exploited to compute semiconductor properties. The solver core has numerous external libraries implemented and tested. A very successful linear kernel was obtained by combining the NAG linear solver library that allows for complex CGS with the permutation and row/column ordering algorithms of Duff and Koster (Harwell Subroutine Library- Hyprotech).

The Finite-Integration Technique uses directly the electric and magnetic field components as basic degrees of freedom. The approach is well established for the simulation of insulators and conductors. However, semiconductors need to be emulated as moderately conducting materials. An original and efficient numerical method called Dual Finite Integration Technique (DFIT), an improved version of FIT, was developed. As in FIT, in the proposed method the global variables are used as DOFs, but unlike the FIT, the Hodge operator is obtained by Galerkin projection, using shape functions, as in Withney (Edge) Finite Element Method. Using both staggered grids as graphs for the electric network and for the magnetic network as well, the new method allows an efficient accuracy control. The dual (complementary) approach allows the effective control of an adaptive procedure for global and local mesh refinement. DFIT accelerates the solution

process, preliminary tests showing that there are 50 times less DOFs needed to obtain the same solution accuracy as in FIT.

To solve real complex problems an original approach called *ALROM (All Level Reduced Order Modeling)* has been developed by LMN. This strategy comprises a series of methods and techniques, which can be applied successively or alternatively in all stages of modeling process. The main idea is to apply each order reduction method as early as possible, in order to keep continuously down the model complexity. In this respect, the electromagnetic simulation is mixed with the order reduction. The ROM techniques and the modeling aspect covered are:

- ***CellHo*** = *Cell Homogenisation* for Non- Manhattan interfaces;
- ***ELOB*** = *Equivalent Layer of Open Boundary* condition - Boundary condition;
- ***dFIT*** = *dual Finite Integrals Technique* - Optimal mesh step;
- ***PROM*** = *Phenomenon based ROM* - eletromagnetic field regime (FW, LL, MQS, EQS, EMQS),
- ***CROM*** = *Coarest ROM based on LEC (Lumped Electric Circuit);*
- ***TCR*** = *Tree/Cotree Reduction*;
- ***FredHO*** = *Frequency Dependent Hodge Operators* - Skin effect;
- ***ASPEEC*** = *Algebraic Sparcified Partial Equivalent Electric Circuit*;
- ***BANESSA*** = *Branch And Node Elimination by Successive Symbolic Approximation*;
- ***(RM) KROM*** = (*Recurrent Multi-point) Krylov based ROM*;
- ***TBR*** = *Truncated Balanced Reduction* - Essential singular values;
- ***VECTORFIT*** = *Frequency Characteristic Fitting* - Frequency behavior.

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In addition to spatial extension addressed by *ALROM* strategy, the simulation method developed by LMN team emphasis also on the speed-up. The simulation strategy called *VFSS* (*Very Fast Simulation Strategy*) comprises besides *ALPROM* (smaller models are obviously simulated faster than large ones) the following acceleration techniques:

- ***TLTM*** - *Transmission Line model based on Transversal Magnetic field*;
- ***AFS*** - *Adaptive Frequency Sampling*;
- ***FTS*** - *Frequencies versus Time domain Simulation*;
- ***PDS*** - *Parallel or Distributed Simulation*.

The capability to turn these methods on and off allows the user to control the CPU time consumption substantially. In particular, a calculation that lasts for a week can be reduced to a few hours.

5. REDUCED - ORDER MODELS

In the first phase of the project (before the test results were available), about 40 problems have been selected for the literature to test and benchmark the theoretical backbone and software implementation.

The rich collection of ROM tools has resulted into the ROM Workbench. The workbench is able to compare the responses obtained for different systems to compare the reference model and the reduced one. The comparison can be carried out either on the time responses (step, impulse, etc.) or on the frequency responses (Bode, Nyquist, Smith, etc). Lumped parameters, quality factors or line parameters can also be compared.

Considering the final aim of the CODESTAR project, i.e. the generation of reduced model synthesized by a SPICE circuit, the ROM workbench includes techniques for circuit synthesis as well. There are two methods implemented. One of them is the Direct Stamping method, more appropriate for reduced models represented by reduced state space matrices (such as the output of Krylov type methods). The other method is the Differential Equation Macromodel, more suitable for reduced order methods that generated transfer functions (such as the output of vector fitting). In this way, the ROM workbench allowed not only the testing of ROM techniques but also of SPICE synthesis algorithms.

From aposteriory methods to reduce the order of Codestar benchmarks, the Vector fitting algorithm proposed by B. Gustavsen and A. Semleyen succeeded the best.

6. IMPLEMENTATION

The Codestar code is a computer program developed in C++ under *Linux OS*. It has a graphical user interface allowing to:

- **define the problem** using a graphical editor;
- **save or load** the problem description in *.xml* file;
- **import** device description from other CAD tools that use standard *.cif* or *.gds2* format for layout and *.sipp* format for technology description;
- **run the field analysis, reduce the order and extract the compact model,** with several options, according to the xml tags in the input file;
- **visualize, evaluate and save the results** in different formats (*.vtk*- visual tool kit, *.sys* - semi-state system, *.snp* - frequency responses in Touchstone format, *.cir* - SPICE netlist).

7. TEST STRUCTURES

The specifications of the test structures were defined in agreement with the end-users, the developers and the characterization engineers. Besides the processing of CMOS (> 100 nm) and BICMOS structures, measurements will be performed on (sub-) 100 nm CMOS devices with integrated back-end passives (RF-CMOS). The structures were characterized using state-of-the-art on-wafer S-parameter measurement techniques. Finally, benchmark simulations were run to evaluate the capabilities and limitations of both commercially available tools and the newly developed tool. IMEC and Austriamicrosystems has provided benchmark reference data for the a series of test cases. Two main groups of test cases have been proposed:

1. **Standard Structures:**
   a. Resistors, Capacitors and Inductors
   b. Transmission line structures in Al/Oxide, Al/Lowk, Cu/Oxide and Cu/Lowk, to cover high frequency applications of advanced interconnect technologies based on Cu and lowk materials and compare them with more traditional materials as Al and oxide;
   c. 2D and 3D interconnect models of current and future technology nodes, based on dimensions and material properties dictated by the ITRS roadmap [1], with the aim of predicting their performance at high frequency.
2. **Challanging Structures** focuses on the implemented test containing guard bars (substrate coupling structures), RF pads and LC oscillators. Again the complete test-chip containing all geometrical and material variations is described and special structures are presented in detail. Those structures are important for RF design and the optimisation is now mainly done by

testchip implementation and subsequent RF measurements. The following structures are implemented on the CODESTAR test-chips

a. LL Cells: The coupling between two identical inductors separated by different distances is examined by these structures

b. LC Cells: The resulting impedance of a capacitor connected in series with a spiral inductor is examined by these structures

c. Substrate coupling analyses structures: The signal at a receptor electrode arrived through the substrate from an injector electrode is examined by these structures.

d. RF – Pads: RF pads provide a low reactance interface point for connecting the internal circuitry through the bond wire and package leads to the application environment.

Full characterisation of the standard structures such as resistors, capacitors and inductors have been done, including intensive discussion of the correct de-embedding strategy. Each measurement plot is completed with a snapshot of the design layout. Only the deembedded part is indicated without the pads and pad interconnects. This is the net geometry the simulations shall be carried on in compliance with the de-embedded measurement data.

8. PROJECT DELIVRABLES

According to the work plan the Codestar project has 19 deliverables, structured in 5 working packages (WP). Following deliverables were developed with important LMN contributions:

WP1 - Solving the field problem:

- **D8** - Report on the usability and adaptation of FIT to solve the field problem (T0+15);
- **D10** - Report on circuit extraction in existing Maxwell solvers (T0+15);

WP2 - Reduced Order Modes:

- **D5** - Report on existing and new order reduction methods (T0+4);
- **D11** - Extraction software library (T0+15);

WP3 - Software implementation:

- **D4** - Report on interface format to the CAD environment (T0+3);
- **D12** - Prototype of software modules (T0+22);
- **D15** - Demonstrator of the final CAD tools (T0+27);

WP4 - Test structures:

- **D1** - Report of end-user requirements (T0+1);
- **D16** - Report on the benchmarking of tools (T0+30)

In each case, in brackets are indicated the deadlines expressed in months.

9. PROJECT ACHEIVEMENTS

The main Codestar achievement is the development of the computer program dedicated to compact models extraction. This code implements the techniques of ALROM and VFS strategies, setting-up a bridge from cif to SPICE. It has following main features:

- **Read** geometry (*layout.cif*) and physical (*technology.sipp*) data;
- The developed code was tested on several benchmark structures including **spiral inductors and interconnects** actually *meander resistors, capacitors, inductors transmission lines and challenging structures*;
- **Large mesh (> 64 000 nodes),** actually, initial virtual meshes *having > 1 million nodes* were used;

- **Imposed accuracy (<5%),** actually *<5% at the standard structures, and <20% in the challenging structures* (less than measurement + technology errors). According D13 the layer thickness have technological errors within 20-76% !! ;
- Large **frequency range: 0 - 10/20 GHz,** actually *0 - 30/40 GHz***;**
- Reasonable simulation time: **< 3 hours**, actually *< 1 hour in the most cases, <160 min. in the challenging cases, without PDS***;**
- Order **reduction from >100 000 to <30 000**, *actually <11 DOFs after final ROM***;**
- **Write** equivalent ***SPICE net-list*** of reduced order model;
- **Matching** between ***measurement and (SPICE) simulation*** results.

The actual *achievements* fulfil the project **commitments**. The Table 1 presents some of numerical results.

Table 1 – Summary of numerical results

Benchmark	**RPOLY 2-ME**	**CMIM**	**SP_SMALL**	**U-COPL AlSiO2**	**SP_COUPL**	**SP_CMIM**
Nodes of initial mesh	368,200	833,280	596,068	2 866 441	681,876	458,304
Initial no. of DOFs	2,209,680	4,999,680	3,576,408	17,198,646	4,091,256	2,749,824
Reduced computational domain	48μ × 43.5μ × 2.937	89.95μ × 89.95μ × 36.814μ	330.45μ × 340.15μ × 195.617μ	200μ × 46.588μ × 17.74μ	1316.5μ × 900μ × 507.497μ	800μ × 800μ × 257.6μ
Nodes of macromodel	5,940	13,440	9614	7,134	10,998	7392
Macromodel DOFs	19,510;	29,925	39920;	19,972	43,138	29862
No. of AFS in (0 -20GHz)	11	15	17	12	15	35
ALLROM CPU time [s]	145	3326	4278	161	2969	9467
Rel. error mes-sim [%]	1.4	2.5	13.6	5.0	15	20
Redced order	4	4	4	10	4	8
Rel.error red-sim [%]	0.16	0.2	0.5	1.3	0.5	0.5

10. DISSEMINATION OF THE PROJECT RESULTS

The dissemination of the project results is made by Internet**: http://www.imec.be/codestar www.lmn.pub.ro/codestar** and through the scientific and technical literature (see reference list, for the LMN contributions). The commercial exploitation of the developed code is made by the spin-off company MAGWEL (**www.magwel.com**). The copyright and project results were registered at "Technological Implementation Plan Desk" (http://etip.cordis.lu – Reduced Order Modeling (ROM) Workbench – IPR for result ID19731).

11. CONCLUSIONS

The Codestar project was for LMN a real breakthrough in the research and development. The methodology for compact model extraction proposed by LMN , based on ALLROM and VFS strategies seems to be the most efficient one, besides those studied within Codestar project. The new powerful extraction technology developed within Codestar project is based on a series of state-of-the-art innovative techniques. However, extension of field modeling to more complex structures requires the solution of following still open problems:

- automatic domain decomposition;
- local adaptive grid refining;
- effective mesh-material decoupling procedures;
- intensive evaluation of new methods (FredHO, ASPEEC, Banessa);
- readable preconditioners for fast iterative solvers;
- parallel solving of large system of linear equations;
- extraction of reduced order state-space models from large, sparse system of DAE;
- robust methods to check and enforce passivity of the extracted compact model;
- synthesis of SPICE circuits with dipolar elements equivalent to compact model.

They will be addressed in next research projects.

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