ATEE-2004

A NEW APPROACH TO THE COMPUTATION OF REDUCED ORDER **CIRCUIT MODELS OF RC CIRCUITS**

F. Constantinescu, A. Gheorghe, C. D. Ioan, M. Nitescu

"Politehnica" University, Bucharest, Romania, Department of Electrical Engineering, e-mail: florinc@ferrari.lmn,pub.ro

Abstract A new method for the computation of a reduced order circuit model, based on numerical elimination of the internal circuit nodes, is presented. The circuit passivity is preserved unlike the majority of other approaches. A 1033 node RC circuit is reduced to an admittance with one pole and two zeros for a frequency range of three decades.

1. INTRODUCTION

In the last years the reduced order circuit models have been proved their usefulness to the fast simulation of electromagnetic field models in integrated circuits. These models are describing interconnection structures as well as passive components. Some specific methods have been developed in the literature: Asymptotic waveform evaluation (AWE) method [1], Complex frequency hopping (CFH) method [2], Padé via Lanczos (PVL) method [3], and PRIMA [4]. A very important feature of this kind of methods is passivity preservation. An order reduction method has this property if any reduced model corresponding to a passive original (high order) circuit is passive. Only one [4] of the known reduced order methods preserves passivity.

The aim of this paper is to analyze the efficiency of the internal node elimination [5,6] as a tool of obtaining reduced order models. Both the symbolic and numerical elimination procedures are considered. A very simple reduced order model of a large scale circuit example is found.

2. INTERNAL NODE ELIMINATION

Writing the equations of a numerical method (finite difference method or finite element method) for solving an electromagnetic field problem in which the inductive effect is negligible is equivalent to the building of a regular structure circuit with branches having a simple structure (for example a parallel RC circuit). The parameter values of these elements depend on the material properties and on the discretization step. Consider a circuit of this kind in Fig.1 having the nodal admittance matrix Y. The circuit equations are YV = J where the entries of V are node voltages and the entries of Y are $y_{ij} = \pm G_{ij} \pm s \cdot C_{ij}$. It follows that the

diagonal

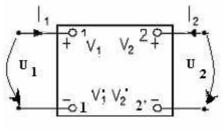


Fig. 1

entries of Y are RC admittances as well as the non-diagonal ones with the minus sign.

A function of the complex variable s is an RC admittance if and only if the following conditions are fulfilled:

- is a rational fraction of s with real coefficients,
- the poles and zeros are simple and alternate on the negative real axis, the closest to the origin being a zero,
- the number of zeros is equal or greater with one with respect to the number of poles.

In order to eliminate all unknowns except V_1 , V_1' , V_2 , and V_2' any circuit equation except the first four can be used. For example, V_p can be eliminated using the equation q in which we

assume that
$$|y_{qp}| \neq 0$$
. It follows: $V_p = -\frac{y_{q1}}{y_{qp}} \cdot V_1 - \frac{y_{q2}}{y_{qp}} \cdot V_2 - \dots - \frac{y_{qn}}{y_{qp}} \cdot V_n$

and each entry of *Y* will be updated as:

$$y_{ij}^{new} = y_{ij}^{old} - \frac{y_{q\,j} \cdot y_{i\,p}}{y_{q\,p}}$$

This is the well known Gaussian elimination and it is used only for the entries for which $|y_{ai} \cdot y_{ip}| \neq 0$ [5,6].

If the node elimination is performed repeatedly using the complex Laplace variable s as a symbol, the expression of the y_{ij}^{new} numerator and denominator become very intricate in a large scale circuit. This is because a simplification procedure is mandatory during the node elimination process. The possibility to build a procedure of this type is analyzed in the following.

The transformation of an intricate RC admittance into a simpler one may be the basis of a passivity preser-

ving algorithm. The following remarks on the node elimination algorithm can lead to some useful conclusions:

• The y_{ij}^{new} computed using a diagonal pivot y_{qp} (q = p) can be an RC admittance; in this

case, if
$$i \neq j$$
, $y_{qq} = G_{qq} + s \cdot C_{qq}$, $y_{qj} = -G_{qj} - s \cdot C_{qj}$, $y_{iq} = -G_{iq} - s \cdot C_{iq}$, $y_{ij}^{old} = -G_{ij} - s \cdot C_{ij}$,

so that $y_{ij}^{new} = y_{ij}^{old} - \frac{y_{RC}^{i} + y_{RC}^{i}}{y_{RC}^{i}}$. y_{ij}^{new} is not necessarily an RC admittance

because the simple pole/zero alternation on the real axis may not be ensured (for example, in a regular structure circuit $y_{RC}^{(1)} = y_{RC}^{(2)}$ and a double zero occurs if $y_{ij}^{old} = 0$.

- For i = j a similar statement can be proved.
- The y_{ij}^{new} computed using an off-diagonal pivot $y_{qp} (q \neq p)$ leads to

$$y_{ij}^{new} = y_{ij}^{old} - \frac{y_{RC}^{(1)} \cdot y_{RC}^{(2)}}{-y_{RC}^{(3)}}$$
 so that y_{ij}^{new} may be, in the best case, a difference of

two RC admittances.

To conclude, the internal node elimination in a regular structure RC circuit used for the electromagnetic field computation doesn't necessarily lead to a circuit made only of RC admittances.

Even though the internal node elimination doesn't lead to a symbolic method for the computation of a reduced order model valid in a certain frequency range, it may be used in

ATEE-2004

numerical computation. As a matter of fact some pivot selection strategies can be developed, each one corresponding to a sparse matrix solving algorithm. To this end some local optimality criteria, as minimum multiplication or minimum fill-in criterion may be used.

As it is well known [8], the symbolic techniques may be more efficient for repetitive computations than the numerical ones if the repetition number exceeds a certain limit. The circuits we are dealing with have smooth frequency characteristics, the frequency range of interest being up to five decades. In this case the numerical methods have a better efficiency. For an one port device the internal node elimination

leads to an admittance connected between the port nodes. It can be proved, using the energy functions [7], that this is a passive RC admittance Y_{RC} . We can compute either the symbolic expression of $|Y_{RC}(\omega)|$ or some values (for certain 's) of it. A procedure giving the reduced order circuit having a given $|Y_{RC}(\omega)|$ within a given error margin w.r.t. the original one is described in the next section. This algorithm preserves the passivity of the original RC circuit. For a two port device the parameters of the voltage controlled representation can be computed by solving two analysis problems:

- 1. Considering $u_1 = 1$ and $u_2 = 0$ we compute $y_{11} = i_1$ and $y_{21} = i_2$.
- 2. Considering $u_1 = 0$ and $u_2 = 1$ we compute $y_{22} = i_2$ and $y_{12} = i_1$.

Knowing y_{11} , y_{22} , and $y_{21} = y_{12}$ the Cauer method of synthesis [7] can be used for finding the reduced order model. Two outstanding properties related to this synthesis method must be taken into account:

- the poles of $y_{21} = y_{12}$ must be poles of y_{11} and of y_{22}
- this method leads to a parallel connection of two ports in Fig.2, each circuit corresponding to a common pole of y_{11} , y_{22} , and y_{21} .

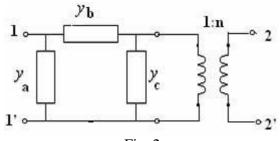


Fig. 2

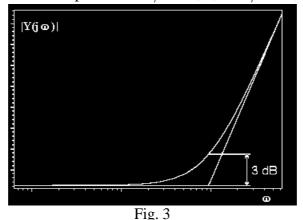
The procedure for finding the reduced order circuit can be outlined as follows:

- solve the field problem for a set of frequencies both for $u_1 = 1$ and $u_2 = 0$ and for $u_1 = 0$ and $u_2 = 1$ and compute $|y_{11}|, |y_{22}|, |y_{21}|$.
- identify the poles of the reduced models of y_{11} and of y_{22} using the method described in the next section with a given
- choose the circuit pole set as a minimal set satisfying the error margin for both y_{11} and of y_{22}
- choose the residue set of y_{21} so that the condition $k_{11} \cdot k_{22} k_{21}^2 \le 0$ be satisfied for each pole
- compute the values n, k_a, k_b, k_c for each two port corresponding to a pole $(y_a = k_a f(s), y_b = k_b f(s), y_c = k_c f(s)$, where f(s) is a simple fraction corresponding to a pole)

ATEE-2004

3. REDUCED ORDER MODEL OF Y_{RC}

The poles and zeros of a RC admittance $Y_{RC}(s)$ alternate on the negative real axis, the closest to the origin being a zero. The shape of the curve $|Y_{RC}(j)|$ vs. is defined by the location of the poles and zeros. Sweeping the axis starting from the origin we remark that the occurence of a zero is associated with a slope change of 20 dB/decade and the occurence of a pole is associated with a slope change of -20 dB/decade [9]. This is because the characteristic $|Y_{RC}(j)|$ has asymptotes whose slopes are 20 dB/decade, 0, 20 dB/decade, 0 a.s.o. Characteristic



approximation by asymptotes has the maximum error of 3dB at the asymptote intersection (Fig.3).

A natural way to approximate $|Y_{RC}(j)|$ is to consider fewer asymptotes with the same slopes as the original ones. The complexity of the reduced model depends on the relative error with respect to the original characteristic. Obviously a greater leads to a simpler reduced model. Our algorithm for finding the reduced order model of a RC circuit has the following steps:

1. computation of the first zero z_1

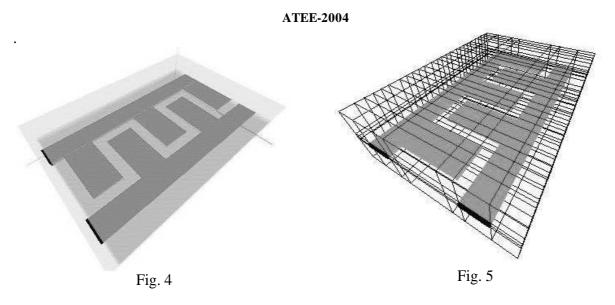
2. computation of the other poles and zeros

3. synthesis of the reduced order circuit

The frequency range of interest is [m, M]. z_1 is set to m. Sweeping the frequency axis with a step m, the error between the asymptote of 20 dB/decade and the given characteristic is checked. The first pole p_1 is placed to the last value before that corresponding to an error of 2 or greater. If this error occurs after the first step m then p_1 is placed very close to z_1 . The first asymptote is translated so that a maximum error of is obtained. The other asymptotes are determined without translation using the condition *error* in each frequency interval corresponding to the given asymptote. Synthesis is performed using a Foster, a Cauer or a Foster-Cauer procedure. By this way a simpler passive RC admittance is obtained, the passivity of the original circuit being preserved.

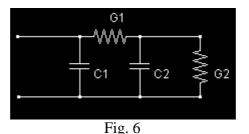
4. EXAMPLE

The case of a regular structure RC circuit resulting from a field problem in a capacitor (Fig. 4) is analysed



A discretization network of 26x8x5 points (Fig.5) leads to a circuit with 1033 nodes, 2801 resistors, and 2801 capacitors. The frequency range of interest is 100MHz - 100 GHz.

Due to the smooth nature of $|Y_{RC}(j)|$ only 15 frequencies are enough, so the numerical AC analysis of PSPICE is used to obtain the frequency characteristic. A program written in the MAPLE language is used to call PSPICE and to compute the reduced model. The input current values are read from the PSPICE file *.*out*. Setting =1.5dB a reduced model with two zeros and one pole is obtained. Using the Cauer I synthesis the circuit in Fig. 6 is obtained.



The parameter values given by MAPLE are:

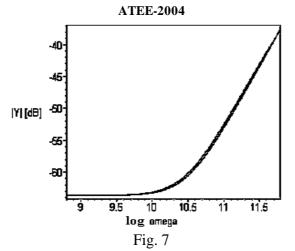
 $C_1 = 0.21256279859459353022 \cdot 10^{-13} R_1 = 1524.1263218120909251$

 $C_2 = 0.50395853046378024786 \cdot 10^{-7} R_2 = 31.664661973608175641$

The frequency characteristic $|Y_{RC}(j)|$ of the original circuit and of the reduced model are given in Fig. 7. The very good agreement between these characteristics is obviously.

5.CONCLUSIONS

The symbolic and numerical internal node elimination is analyzed in order to be used for building the reduced order circuit models. The large scale passive RC circuits arising in the numerical electromagnetic field computation are taken into account. The symbolic elimination produces intricate expressions for which a simplification procedure which preserves passivity has not been found.



The numerical internal node elimination is equivalent to known sparse matrix methods and can be used to compute the frequency characteristics in the range of interest. An algorithm for the synthesis of a reduced model of a one port or two port structure has been presented. This algorithm includes a very simple simplification procedure for a passive RC admittance based on the pole-zero pattern and on the 0 dB/dec and 20 dB/dec asymptotes.

A reduced model containing four circuit elements has been built for a circuit with 1033 nodes, 2801 resistors, and 2801 capacitors.

The future work will address the reduced models of the RLC circuits with coupled coils arising in numerical solving of the electromagnetic field problems where the inductive effect is not negligible.

Acknowledgement The authors would like to thank the support received from the FP5 project CODESTAR.

References

[1] L. T. Pillage, R. A. Rohrer, "Asymptotic waveform evaluation for timing analysis", *IEEE Trans. on Computer -Aided Design of Integrated Circuits and Systems*, vol.9, April 1990.

[2] E. Chiprout, M. Nakhla, "Analysis of interconect ntworks using complex frequency hopping", *IEEE Trans.* on Computer -Aided Design 14: 186-199, 1995.

[3] P. Feldmann, R.W. Freund, "Eficient linear circuit analysis by Padé approximation via the Lanczos process", *computer Society Press 1994.*

[4] A. Odablasioglu, M. Celik, L.T. Pillage, "PRIMA: Passive-Reduced-Order Interconect Macromodeling Algorithm", *IEEE Trans. on Computer -Aided Design of Integrated Circuits and Systems*, 17(8): 645-653, 1998.

[5] M. Pierzchala, B. Rodanski, "Generation of sequential symbolic network functions for large-scale networks by circuit reduction to a two-port," *IEEE Trans. o n Circuits and Systems - I: Fundamental Theory and Application* s, vol. 48, no. 7, July 2001, pp. 906-909.

[6] B. Rodanski, "Computational Efficiency of Symbolic Sequential Formulae," *Proc. SMAC* D, Lisbon, Portugal, October 2000, pp. 45-50.

[7] A. Mateescu, Circuit Analysis and Synthesis, Didactical and Pedagogical Publishing House, 1975 (in Romanian).

[8] M. Nitescu, F. Constantinescu, Symbolic vs. numerical methods for solving repetitive computation problems, SMACD'96, Leuven, Belgie, October 9-11, 1996.

[9] P. R. Gray, P.J. Hurst, S. H. Lewis, R., G. Meyer, Analysis and design of analog integrated circuits, John Wiley & Sons, 2001.