REDUCED-ORDER MODELLING TECHNIQUES BASED ON STATE VARIABLE SPACE AND THEIER USE IN CIRCUIT DIAKOPTIC ANALYSIS

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Abstract. In this paper we present some new tearing techniques to systematically formulate the state equations in symbolic normal-form for linear and/or nonlinear time-invariant large-scale analog circuits. The excess elements of the first and of the second kind are unitarily treated in order to allow a symbolic representation of the circuit with a minimum number of state variables. It is also presented a procedure to reduce, for each subcircuit, the state equation number. The reduced-order is based on the using of an implicit integrated algorithm and on the successive elimination of the imposed state variables. Some examples are given to illustrate the decomposition procedure, the assignment of the connection sources and the reduce-order techniques.

I. INTRODUCTION

The growth in complexity of IC chips has generated the need for more efficient simulation techniques, which radically differ from the standard simulation techniques [1,2,3,4].

There are two fundamental approaches for coping with increasing sizes of electronic circuits:

1. **Circuit decomposition**, i.e., partitioning the given circuit into smaller component circuits which can be handled easily;
2. **Macromodelling and macroanalysis**, which imply simplification of the transistor models and/or writing of some global equations describing the input/output behavior of a subcircuit.

The earliest technique proposed to handle large-scale circuits by decomposition is called *diakoptics* or *tearing*.

A tearing method implies "tearing apart" or decomposing a large-scale network into a number of smaller circuits – called *subcircuits*, which are processed independently. Each subcircuit matrix is then operated upon, together with the appropriate topological matrices, to yield the overall solution. As a consequence, a reduction of the operation number and hence of the computing time is achieved.

Advantages of the decomposition techniques are of two types:

1. The development of parallel processing systems for solving several subcircuits simultaneously leads to a reduction in computation time;
2. Solving only the non-latent subcircuits sequentially in the proper order using the latency principle yields savings in computation time and memory space.

In the last years some new algorithms and computer programs have been developed in this area in order to be used in CAD of analog integrated circuits. Design problems as noise analysis, sensitivity computation, distortion analysis of weakly nonlinear circuits, symbolic pole/zero extraction, circuit sizing based on optimization of analytic models can be efficiently solved by means of symbolic methods [3,4]. The hierarchical analysis using graph decomposition [5,6], matrix decomposition [7], or splitting of the circuits containing nullors [8,9], leads to significant reduction of CPU time.

The decomposition of a large-scale analog circuit into a number of smaller subcircuits can be made by:

- *branch tearing* [2,7-13], in which appropriate branches are removed;

- *node tearing*, in which the circuit is torn apart along appropriate nodes [2,7-18];
- *node and branch tearing*, in which the circuit is torn apart along appropriate nodes and appropriate branches are removed [2,9-13,19,25];
- *splitting of some central nodes* from the normal tree [13,14,19].

In this paper we present three tearing techniques from the last category of decomposition methods, which can be applied both for linear and/or nonlinear large-scale analog circuits.

Remark 1. In the case of the nonlinear circuits, because the numerical differentiation is a relatively inaccurate operation, we approximate the $q_k - v_k$ characteristic of each nonlinear capacitor and the $\varphi_k - i_k$ characteristic of each nonlinear inductor by piecewise-linear segments. In order to simplify the description of nonlinear resistors, their $v - i$ characteristics may be approximated by piecewise-linear continuous curves, or by new characteristics in which the nonlinearities are transferred to the sources, [12,13,14,17,19,20,22,26,28].

Remark 2. Using the state equations in symbolic form, we obtain a significant efficiency in circuit design and an improvement of the accuracy in the numerical calculations by considering as symbols only the parameters corresponding to the nonlinear circuit elements. By symbolic analysis, the coefficients of the characteristic polynomial can be computed exactly, in order to evaluate the eigenvalues. In this way it is easy to estimate the time step as a fraction of the smallest time constant (the inverse of the largest real part of an eigenvalue). The total simulation time to reach the steady state may be estimated as few times the largest time constant (the inverse of the smallest nonzero real part of an eigenvalue) [28].

Remark 3. If the circuits contain magnetic couplings, we can simulate them by inductors and current derivative-controlled voltage sources [12,17,27,28].

The tearing techniques developed in the Section II of the paper allow the systematic formulation of the state equations in symbolic normal-form, for linear and/or nonlinear time-invariant large-scale analog circuits with excess elements. The degenerates of the first and of the second kind are unitarily treated in order to allow a symbolic representation of the circuit with a minimum number of state variables, and to identify the null eigenvalues. The decomposition algorithm was implemented in a computing program [19] that automatically generates the symbolic state equations.

Using an implicit integrated algorithm to integrate numerically the state equations we can reduce the state equation number by elimination of the imposed state variables. Solving a reduced algebraic equation number yields savings in computation time and memory storage.

The algorithm for writing the symbolic state equations using the circuit decomposition and the procedure to reduce, for each subcircuit, the state equation number are given in Section III. Section IV contains three illustrative examples, including diakoptic analysis of the opamp μA741 using a symbol set for which the analysis of the whole circuit is not possible.

II. TEARING TECHNIQUES FOR STATE EQUATION FORMULATION

In order to formulate the circuit state equations, a normal tree of the circuit is selected. This is a special tree which contains certain circuit elements in the following priority order: all independent and controlled voltage sources, all nonlinear voltage-controlled resistors, as many capacitors as possible, as many controlling branches of the current-controlled voltage sources and of the current-controlled current sources as possible (these branches are considered as resistive branches having null resistances), as many resistors as possible, and as few inductors as possible. It does not contain any independent and/or controlled current source, and any nonlinear current-controlled resistor. The capacitors that are not included in the normal tree are called *excess capacitors*, and the inductors that are included in the normal tree are called *excess inductors*.

The nodes of the normal tree in which at least two tree branches and as much as links are connected, are called *central nodes*, and those in which only one tree branch is connected are called *external nodes*.

In the following we present a decomposition procedure of a large-scale circuit by splitting of some central nodes from its normal tree. All tearing methods require that the elements in a subcircuit must be strongly interconnected, whereas the different subcircuits must be weakly interconnected [2,15,16,30] each other. We have to choose p central nodes, which are considered as *reference nodes*. These p reference nodes are torn apart by *p splitting cut-sets* (SCS) into $p + 1$ subcircuits. As we shall show below, in respect to the reference node of each splitting cut-set, we define the connection sources.

There are three possible ways to tear the large-scale circuit into subcircuits: 1) *by nodes*: the reference nodes and other nodes are torn apart as in Fig. 1; 2) *by nodes and branches*: the reference nodes are torn apart and several branches are sectioned; 3) *hybrid*: the reference nodes and other nodes are torn apart and several branches are sectioned.

Remark 4. Through the same central node can pass one, more or all splitting cut-sets.

Any splitting cut-set generates two subcircuits. In all tearing variants the p+1 subcircuits can be interconnected either by ideal independent voltage sources (e_{con}) and ideal independent current sources (j_{con}) (independent connection sources) or by VCVS's with unity voltage gain and CCCS's with unity current gain (controlled connection sources).

Since a subcircuit contains the same modeling primitives as the original circuit (that will be restored finally by reconnecting all the subcircuits), the accuracy of the simulation results is not affected.

Remark 5. The assignment of the connection sources to the subcircuits has to keep, as much as possible, the structure of the state variable vector of the whole circuit.

Remark 6. The independent or controlled connection voltage sources do not have to generate loops made up only of voltage sources. Also, the independent or controlled connection current sources do not have to determine cut-sets made up only of current sources.

We call circuits with excess elements [2,12,13,16,22,25,28], (the circuits with degenerates of the first kind) the circuits containing:

- Loops of capacitors and independent and/or controlled voltage sources (*C-E* loops);
- Cut-sets of inductors and independent and/or controlled current sources (*L-J* cut-sets).

The cut-sets of capacitors and independent and/or controlled current sources (*C-J* cut-sets) and the loops of inductors and independent and/or controlled voltage sources (*L-E* loops) determine dependencies among capacitor voltage derivatives and inductor current derivatives (the degenerates of the second kind). In this case, each *C-J* cut-set and/or each *L-E* loop introduces a null eigenvalue, [5,13,19].

When by the assignment of the connection sources *C-E* loops and/or *L-J* cut-sets appear, the currents of connection voltage sources and the voltages of the connection current sources depend also on the derivatives of the state variables of these subcircuits. In this case, in order to obtain the state equation in normal form for the whole circuit, we have to solve the system having as unknowns the derivatives of all state variables.

To avoid this situation we can insert in series with each e_{con} and/or each VCVS, belonging to a *C-E* loop, a small resistance (having a value of 10^3 smaller than the smallest circuit resistance). Similarly, a big resistance (having a value of 10^3 bigger than the biggest circuit resistance) can be connected in parallel with each j_{con} and/or each CCCS, belonging to an *L-J* cutset. These resistors simplify the computation of the currents (voltages) of the e_{con} (j_{con}) in respect of the state variables and the input variables of the corresponding subcircuits. On the other hand they introduce new eigenvalues having the magnitudes much bigger than the biggest magnitude of the circuit eigenvalues.

When independent connection sources are used, the currents and the voltages of the ideal independent voltage sources and of the ideal independent current sources must satisfy, at each splitting cut-set Σ_k, $k=\overline{1,p}$, the following relations:

$$\begin{aligned} i_{econ,k} &= j_{con,k}, \\ e_{con,k} &= v_{jcon,k} \end{aligned}. \tag{1}$$

If controlled connection sources are used, they must satisfy the controlling equations:

$$\begin{aligned} e_{con,k} &= 1 \cdot v_{jcon,k}, \\ j_{con,k} &= 1 \cdot i_{econ,k} \end{aligned}. \tag{2}$$

In this case, because the controlling variables of the controlled sources must belong to the state vector or to the variable vector associated to the resistors, we have to do some modifications in the circuit structure. We must insert a very small resistance (a very large resistance) in series (in parallel) with each connection VCVS (with each connection CCCS). Obviously, if there is another circuit element connected in parallel with each connection CCCS, we do not have to introduce a very large resistance in parallel with, any more.

The two subcircuit interconnection variants imply different way to obtain the state equations of the entire circuit.

So, when independent connection sources are used, the subcircuits are separately processed, and finally, by aggregation of the state equations of all subcircuits (that suppose the elimination of the connection sources) the whole circuit solution is obtained. For the large-scale integrated circuits' analysis, the parallel processing can be used.

In the second case, when controlled connection sources are used, we have to solve the complete state equation system from the beginning, but the equations are much better structured.

III. SETTING UP THE SYMBOLIC STATE EQUATIONS

After the generation of a circuit normal tree, the essential incidence matrix (*EIM*) $\boldsymbol{D}_m$, associated to the normal tree in the subcircuit S_m, is generated with the following partition

$$\boldsymbol{D}_m = \begin{array}{c} \\ E_{i,m} \\ E_{c.m} \\ E_{con.m} \\ C_{t,m} \\ R_{t,m} \\ L_{t,m} \end{array} \begin{array}{c} \begin{array}{cccccc} C_{l,m} & R_{l,m} & L_{l,m} & J_{c,m} & J_{i,m} & J_{con,m} \end{array} \\ \begin{bmatrix} \boldsymbol{D}_{E_iC.m} & \boldsymbol{D}_{E_iR,m} & \boldsymbol{D}_{E_iL,m} & \boldsymbol{D}_{E_iJ_c,m} & \boldsymbol{D}_{E_iJ_i,m} & \boldsymbol{D}_{E_iJ_{con},m} \\ \boldsymbol{D}_{E_cC.m} & \boldsymbol{D}_{E_cR.m} & \boldsymbol{D}_{E_cL.m} & \boldsymbol{D}_{E_cJ_c.m} & \boldsymbol{D}_{E_cJ_i.m} & \boldsymbol{D}_{E_cJ_{con}.m} \\ \boldsymbol{D}_{E_{con}C.m} & \boldsymbol{D}_{E_{con}C.m} & \boldsymbol{D}_{E_{con}L.m} & \boldsymbol{D}_{E_{con}J_c.m} & \boldsymbol{D}_{E_{con}J_i.m} & \boldsymbol{D}_{E_{con}J_{con}.m} \\ \boldsymbol{D}_{CC.m} & \boldsymbol{D}_{CR.m} & \boldsymbol{D}_{CL.m} & \boldsymbol{D}_{CJ_c.m} & \boldsymbol{D}_{CJ_i.m} & \boldsymbol{D}_{CJ_{con}.m} \\ \boldsymbol{0} & \boldsymbol{D}_{RR.m} & \boldsymbol{D}_{RL.m} & \boldsymbol{D}_{RJ_c.m} & \boldsymbol{D}_{RJ_i.m} & \boldsymbol{D}_{RJ_{con}.m} \\ \boldsymbol{0} & \boldsymbol{0} & \boldsymbol{D}_{LL.m} & \boldsymbol{D}_{LJ_c.m} & \boldsymbol{D}_{LJ_i.m} & \boldsymbol{D}_{LJ_{con}.m} \end{bmatrix} \end{array} \tag{3}$$

where, for example, $E_{i,m}$ ($J_{c,m}$) is the set of independent (controlled) voltage (current) sources from the subcircuit S_m, and $\boldsymbol{D}_{CC,m}$ $(\boldsymbol{D}_{LL,m})$ represents the incidence submatrix of the link capacitors (inductors) to the cut-sets associated to the tree branch capacitors (inductors) from the subcircuit S_m. The existence of the null matrices $\boldsymbol{D}_{RC,m}=\boldsymbol{0}$, $\boldsymbol{D}_{LC,m}=\boldsymbol{0}$, $\boldsymbol{D}_{LR,m}=\boldsymbol{0}$ is a consequence of the normal tree definition [2-6,9,13,15].

Using the second-level subscript *t* for the normal tree branches, and *l* for the links (cotree), the Kirchhoff's laws have the form:

KCL: $$\boldsymbol{i}_{t,m} = -\boldsymbol{D}_m \boldsymbol{i}_{l,m} \tag{4}$$

KVL: $$\boldsymbol{v}_{l,m} = \boldsymbol{D}_m^{\mathrm{t}} \boldsymbol{v}_{t,m}, \tag{5}$$

where, for example, $\boldsymbol{v}_{t,m}\,(\boldsymbol{i}_{l,m})$ represents the voltage (current) vector of the tree branches (links).

To this equation system we must add the constitutive equations of the linear and/or nonlinear circuit elements, and the definition equations of the controlled sources. We assume that the voltages of the controlled voltage sources, $\boldsymbol{v}_{E_c,m}$, and the currents of the controlled current sources, $\boldsymbol{i}_{J_c,m}$, can be expressed in respect of the resistor voltages or the resistor currents, or the state variables.

The number of state-variables associated with the circuit being equal to the number of dynamic elements minus the number of excess elements, [1,2,9,11-14,18-23], we choose as state variables the tree capacitor voltages $\boldsymbol{v}_{Ct,m}$ and the link inductor currents $\boldsymbol{i}_{Ll,m}$. The complete equation system must be solved in respect of these variables.

According to the algorithm presented in [31], the symbolic state equations in normal form, for the subcircuit S_m, are:

$$\dot{\boldsymbol{x}}_m = \boldsymbol{A}_m \boldsymbol{x}_m + \boldsymbol{B}_m \boldsymbol{y}_m + \boldsymbol{B}_{1,m} \dot{\boldsymbol{y}}_m \tag{6}$$

where the matrices $\boldsymbol{A}_m$, $\boldsymbol{B}_m$ and $\boldsymbol{B}_{1,\mathrm{m}}$ have the elements in symbolic form, and

$$\boldsymbol{x}_m = \begin{bmatrix} \boldsymbol{v}_{Ct,m}^{\mathrm{t}} & \boldsymbol{i}_{Ll,m}^{\mathrm{t}} \end{bmatrix}^{\mathrm{t}}, \qquad \boldsymbol{y}_m = \begin{bmatrix} \boldsymbol{v}_{E_i,m}^{\mathrm{t}} & \boldsymbol{v}_{E_{con},m}^{\mathrm{t}} & \boldsymbol{i}_{J_i,m}^{\mathrm{t}} & \boldsymbol{i}_{J_{con},m}^{\mathrm{t}} \end{bmatrix}^{\mathrm{t}}. \tag{7}$$

The vectors $\boldsymbol{v}_{E_{con},m}$ and $\boldsymbol{i}_{J_{con},m}$, $m = \overline{1,p+1}$, must be expressed in respect of all state variables, of the voltages of all independent voltage sources, and of the currents of all independent current sources. For that, we use the Kirchhoff's current law corresponding to the cut-sets attached to the connection voltage sources, and the Kirchhoff's voltage law corresponding to the loops attached to the connection current sources, obtaining for each subcircuit S_m, $m = \overline{1,p+1}$.

Because the two connection sources ($e_{con,k}$, $j_{con,k}$) attached to a splitting cut-set Σ_k are assigned to different subcircuits (S_{m-1} and S_m), they must satisfy the following relations:

$$\boldsymbol{i}_{E_{con},m-1} = \boldsymbol{i}_{J_{con},m} \tag{8}$$

$$\boldsymbol{v}_{J_{con},m} = \boldsymbol{v}_{E_{con},m-1}. \tag{9}$$

By the aggregation of the equations for all subcircuits we obtain the state equation in symbolic form for the whole circuit:

$$\dot{\boldsymbol{x}} = \boldsymbol{A}\boldsymbol{x} + \boldsymbol{B}\boldsymbol{y} + \boldsymbol{B}_1 \dot{\boldsymbol{y}} \tag{10}$$

where the matrices $\boldsymbol{A}$, $\boldsymbol{B}$ and $\boldsymbol{B}_1$ have the elements in symbolic form.

In order to integrate the state equation (6) we use the backward-differentiation formula [22], which approximates to within prescribed accuracy the present value $\dot{x}(t_{n+1}) = \dot{x}_{n+1}$ of the time derivative of $x(t_{n+1}) = x_{n+1}$ in terms of x_{n+1} and p past values $x_n, x_{n-1}, \ldots, x_{n-p+1}$:

$$\dot{x}_{n+1} = \frac{1}{h}\sum_{k=0}^{p} a_k x_{n+1-k} = \frac{1}{h}\left(x_{\_n} - x_{\_o}\right), \tag{11}$$

where: $a_0, a_1, \ldots, a_p$ are constants, $h = t_{n+1} - t_n$ is the present step size, $x_{\_n} = a_0 x_{n+1}$ is the new value of x, and $x_{\_o} = \sum_{k=1}^{p} a_k x_{n+1-k}$ is the "old" value of x.

According to the relation (14) the state equation (6) becomes:

$$\frac{1}{h}\left(\boldsymbol{x}_{m\_n} - \boldsymbol{x}_{m\_o}\right) = \boldsymbol{A}_m \boldsymbol{x}_{m\_n} + \boldsymbol{B}_m \boldsymbol{y}_{m\_n} + \boldsymbol{B}_{1,m} \frac{1}{h}\left(\boldsymbol{y}_{m\_n} - \boldsymbol{y}_{m\_o}\right). \tag{12}$$

Solving the equation system corresponding to the eliminated state variables and introducing them in the remained state equations, we obtain the state equations in the normal form for the remained state variables. These state equations have the form similar to the equation (12) and have as symbols the old values of all state variables and time step size. The remained state equations can easy be integrated to obtain the circuit response. With this method we obtain important savings in computing time and memory.

The method we developed can be used to obtain the transfer function if the kept state variable is that of the output port. The approach is tested on some very important analog integrated circuits of practical interest.

The algorithm for large-scale circuit decomposition, and the method to systematically formulate the state equations in symbolic normal-form for linear and/or nonlinear time-invariant large-scale analog circuits with excess elements, was implemented in **SYSEG** – **SY**mbolic **S**tate **E**quation **G**eneration- program. Starting from the circuit netlist, the program performs the decomposition of the large-scale analog circuit into $p + 1$ subcircuits, identifying the p splitting cut-sets, and formulates the state equations in symbolic form. It follows the algorithm of the symbolic formulation of the state equation in normal form, but it avoids the matrices' multiplication. Kirchhoff's laws are simple written by successively generation of the cut-sets and of the loops respectively, that makes the program very efficient regarding the computing time and memory. The program SYSEG is written in C++ language and it is implemented on a compatible IBM Pentium PC. This is an interactive tool that combines symbolic and numeric computational techniques and which uses the facilities of symbolic simulator Maple to manipulate the symbolic expressions.

IV. EXAMPLE

The diakoptic approach leads to a significant reduction of CPU time and an important economy of memory, in contrast with the case when the analysis is made over the entire circuit. When the symbolic analysis of the whole large-scale circuit is not possible, the tearing method becomes the unique alternative and this is its main advantage.

A good example is the μA 741 operational amplifier, shown in Fig.1, whose partially symbolic state equations in normal form we want to formulate, in order to extract the circuit state matrix.

Applying our computing program [19] we can obtain the symbolic state equations in normal form for different number of symbols and for different locations of the corresponding circuit elements.

In some situations, though, the symbolic expressions being too large, the symbolic manipulator fails [20]. This happens, for example, when we take as symbols the parameters of the transistors Q_4, Q_{131}, Q_{16}, Q_{17}, Q_{21}, and R_8, R_9, R_{11}, C_1. If the transistors are modeled as in Fig. 2, the small-signal equivalent circuit of the amplifier in open-loop configuration contains 26 nodes and 140 primitive elements. We have performed a diakoptic analysis tearing the circuit by Σ_1, Σ_2, and Σ_3 cut-sets, in four subcircuits.

These were independently analyzed, and the partially symbolic state equations of the entire circuit, with 36 symbols (including the six connection resistances, and the complex frequency s), were obtained by aggregation. The numerical values of the eigenvalues obtained by the numeric analysis of the whole circuit are in a good agreement with those obtained by symbolic diakoptic analysis (see Fig.3). The maximum error is 5.14% for a complex conjugate eigenvalue that can be seen in the figure.

Eliminating the state variables:

Elm_st_var:=[UCbe_Q17,UCbe_Q5,UCbe_Q12,UCbe_Q19,UCbc_Q1,UCbe_Q20,UCbe_Q15,UCbc_Q16, UCbe_Q10,UCbc_Q131]],

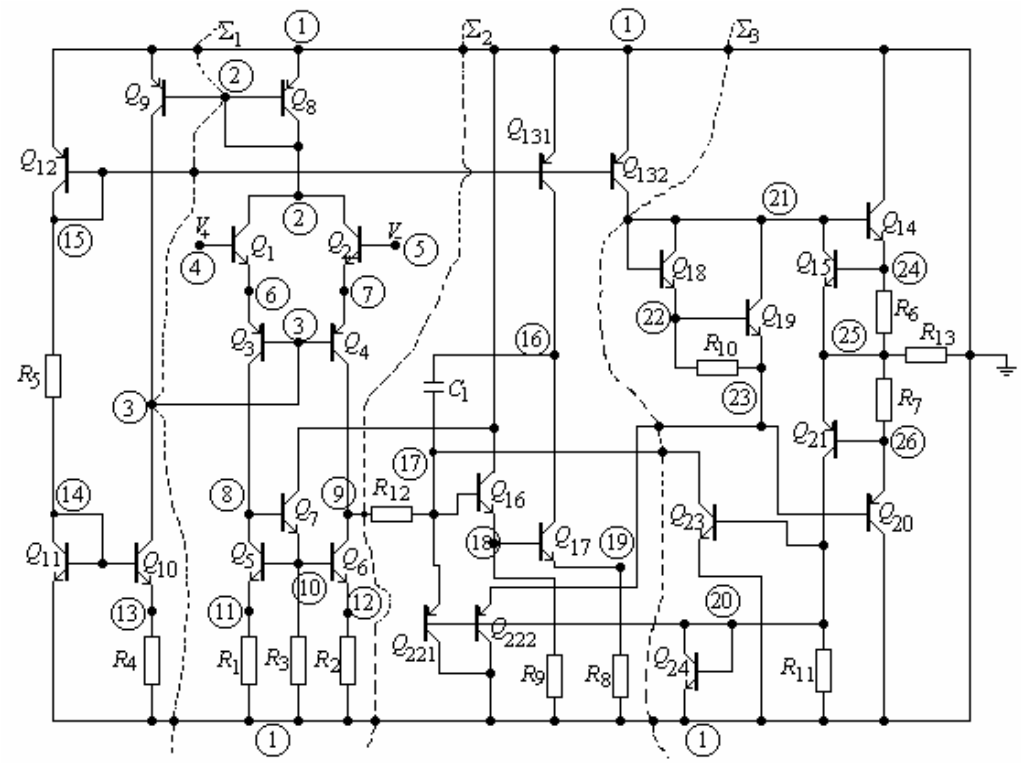

Fig.**1.** μA741 operational amplifier.

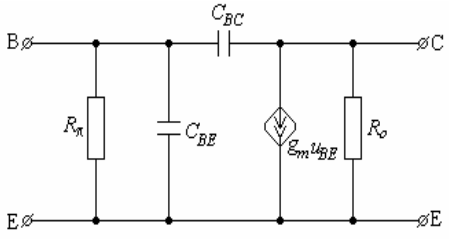

Fig.**2**. AC model for bipolar transistors.

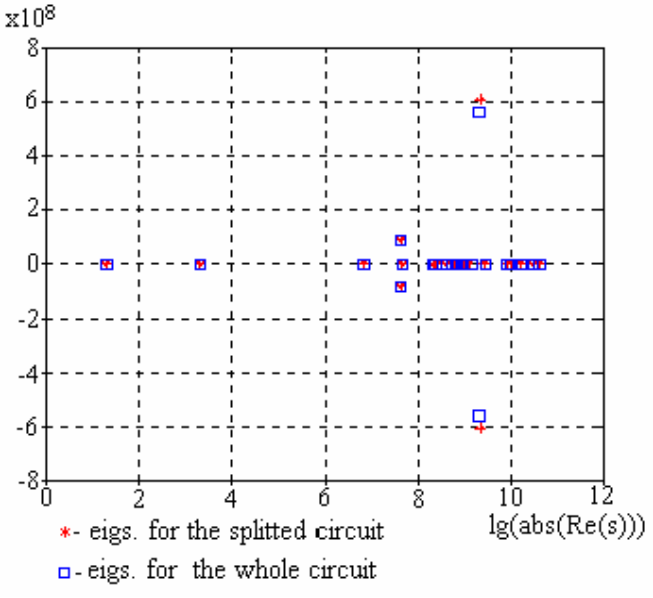

Fig. **3.** Pole location for μA 741.

The first two remained state equations, for *h* = 1e-14, have the following numeric structure:

Rem_st_eqs:={.1e15*UCbe_Q6_n-.1e15*UCbe_Q6_o = -.8750e9*UCbe_Q6_n+
+.3335e5*UCbc_Q4_n-.3335e5*UCbc_Q3_n+.6803e9*UCbc_Q5_n+.
+6803e9*UCbc_Q7_n,

.1e15*UCbe_Q18_n-.1e15*UCbe_Q18_o = -.1065e9*UCbc_Q3_n+

+.1065e9*UCbc_Q4_n-.2250e9*UCbe_Q12_o+.6875e9*UCbe_Q15_o+
4282e9*Cbc_Q16_o-.5659e10*UCbe_Q19_o-.3442e9*UCbe_Q16_n-.3055e9*
*UCbe_Q17_o-.4344e10*UCbe_Q18_n-.4109e10*UCbe_Q20_o-
-.2658e6*UCbc_Q21_n+.1926e5*UCbc_Q10_n+
+.5963e9*UCbc_Q131_o-.1065e9*UCbc_Q7_n+.5017e10*UCbe_Q14_n-
-.5678e9*UCbc_Q132_n}

V. CONCLUSION

Based on the topological method of the normal tree we have developed a very efficient algorithm to generate in symbolic form the state equations of the analog circuits with excess elements. In order to extend this very useful method to the large-scale integrated circuits design, we have developed several tearing techniques, based on splitting of some central nodes (called reference nodes) from the normal tree. These techniques are built on three variants of circuit decomposition: by nodes (reference nodes and other nodes), by nodes and branches (reference node and several branches), and hybrid (by reference nodes, other nodes and several branches). Because an optimal decomposition needs that the elements of a subcircuit must be strongly interconnected, while the subcircuits must be weakly interconnected each other, and also the subcircuits must have equal sizes, the choice of one tearing method or another one depends on the circuit structure and on these requirements.

The choice of the values of these resitances depends on the circuit structure and on the values of the resitances contained in the initial circuit. The connection resistors introduce new eigenvalues that have the magnitudes much bigger than the biggest magnitude of the circuit eigenvalues, and that do not affect the dynamic behavior of the circuit.

The main advantage of the diakoptic approach is that it can be used in the cases when the symbolic analysis of the whole circuit is not possible.

The reduced-order of the number of the state variables, based on the using of an implicit integrated algorithm and on the successive elimination of the imposed state variables, is an efficient procedure for the simulation of the large-scale integrated circuits.

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